



fab materials and patterning challenges for future IC technologies

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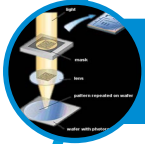
Agenda



Moore's Law in 2018+



Keys to Success in Semiconductor Supply Chain



Patterning Challenges in Advanced Logic & 3D-NAND



Summary

*"The number of transistors and resistors
on a chip doubles every 24 months"*

-Gordon Moore

Two Implications:

1. Cost per square millimeter goes up over time
2. Doubling of transistors = "Scaling"
 - Improves performance
 - Cost per transistor declines

WHAT IF MOORE'S LAW IS APPLIED TO...

TRANSPORTATION?



We could travel to the Sun on a single gallon

AGRICULTURAL PRODUCTIVITY?



We could feed the world's population with 1km² of land

SPACE TRAVEL?

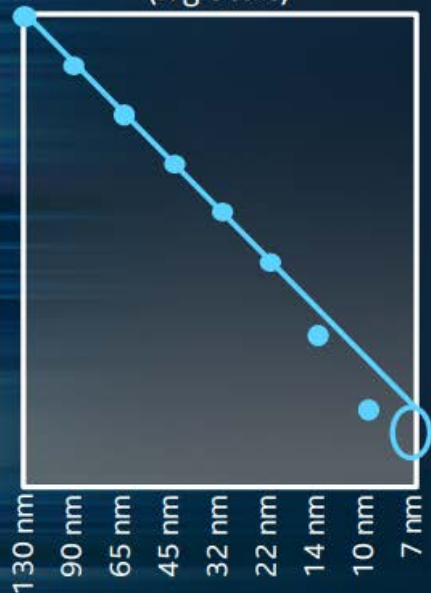


We could travel at 300x light-speed

Source: Intel estimates.

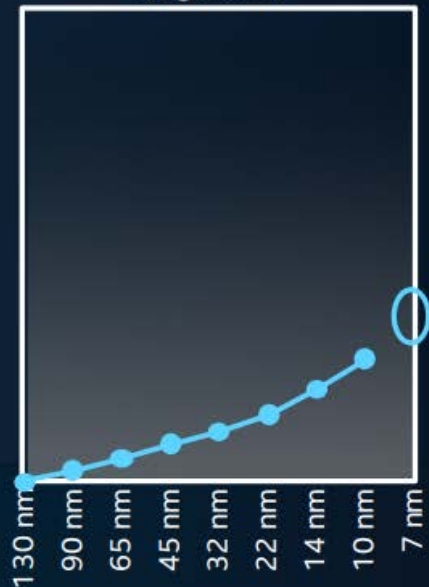
IS MOORE'S LAW DEAD? NO!

mm² / Transistor
(log scale)



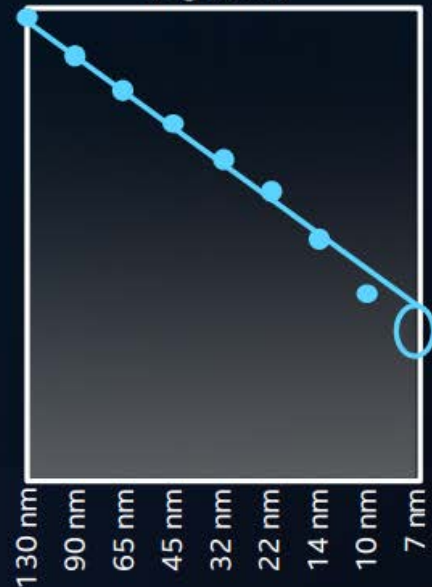
×

\$ / mm²
(log scale)



=

\$ / Transistor
(log scale)

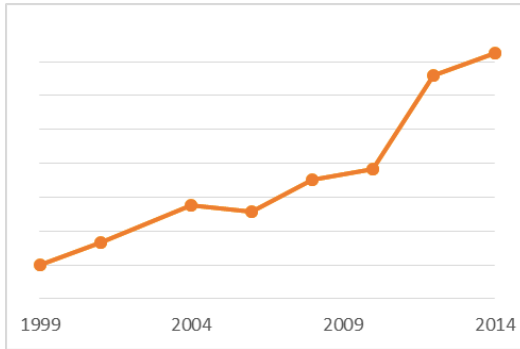


10 nm and 7 nm forecasts are Intel estimates, based upon current expectations and available information.
Source: Intel

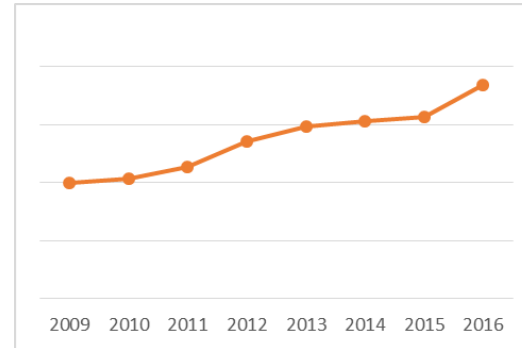
Keys to Success in the Semiconductor Supply Chain

Semiconductor technology progression is as much about **changes in materials** as it is about **line width scaling**.

New materials per technology have increased **600%** in the past **17 years**.

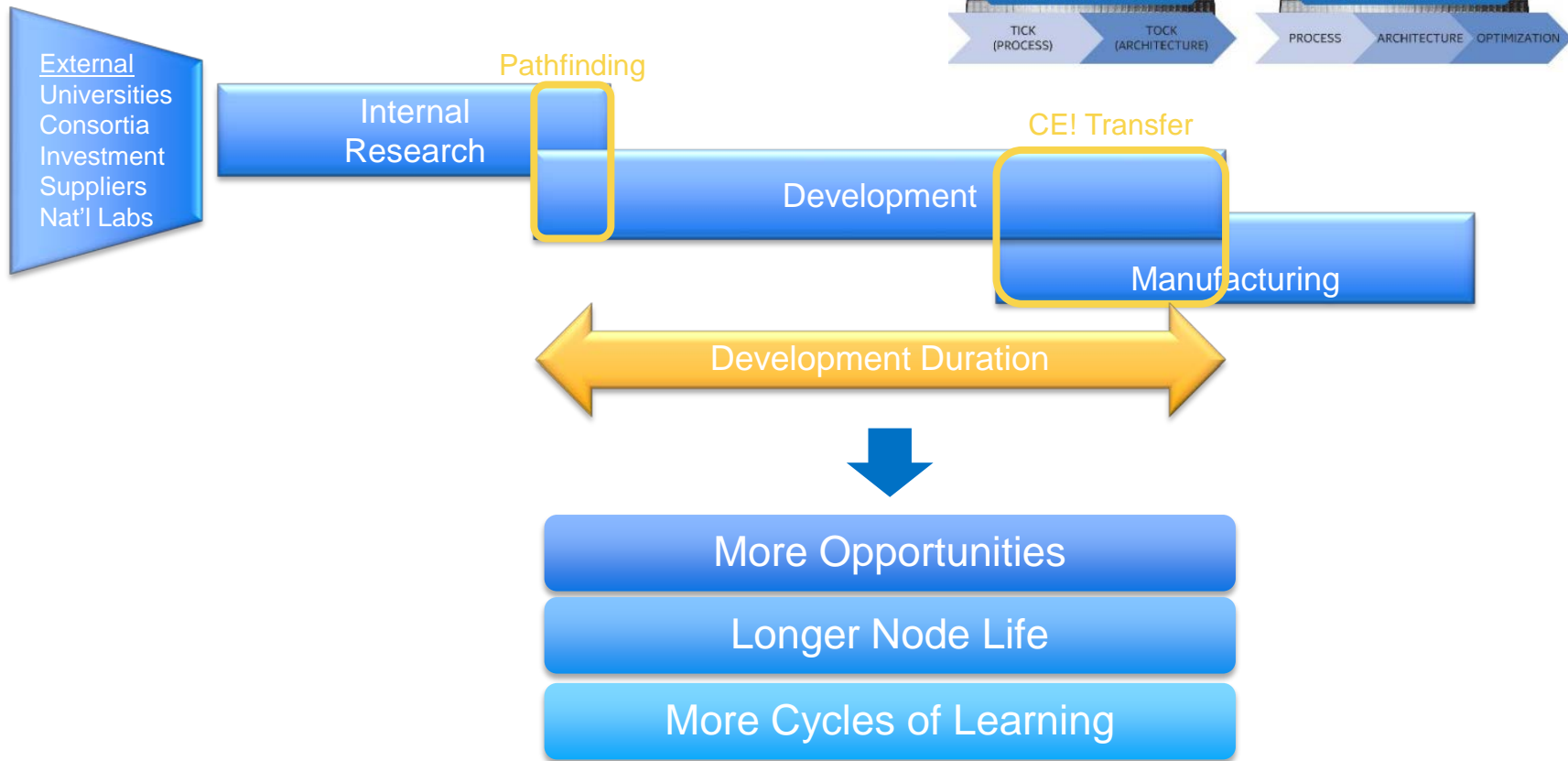


The number of active raw material part numbers increased almost **85%** in the past **7 years** alone.



New materials mean more suppliers, more sub-suppliers, and increase the importance of effective **Supply Chain management**.

Intel's R-D-M Model



What does Intel look for in our Suppliers?

C

Cost



Q

Quality



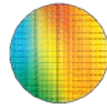
A

Availability



T

Technology



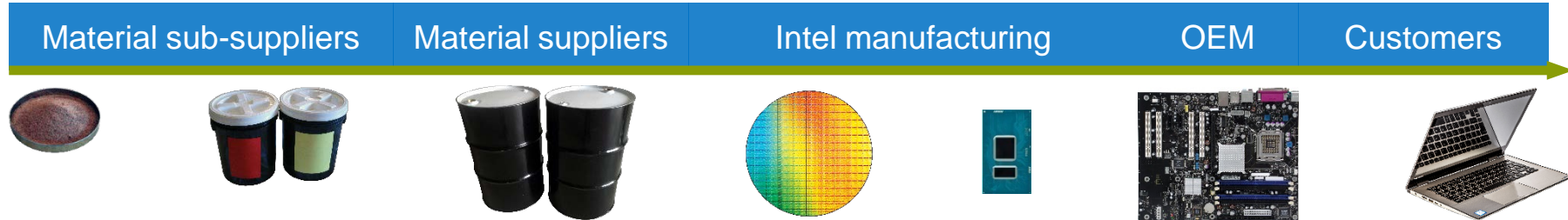
S

Sustainability



Successful Suppliers perform well in all areas

Intel's supply chain spans from our
suppliers' **sub-suppliers** to our customers' **customers**.



Small problems not prevented early
increase exponentially in impact
as value is added in the supply chain.



We need **your help** to drive these
9 quality elements
into the **supply chain.**



Maintain
**change
control**

Track
**process
control**

Use robust
**supplier
selection**

Control
**incoming
material
quality**

Trace and contain
**non-conforming
material**

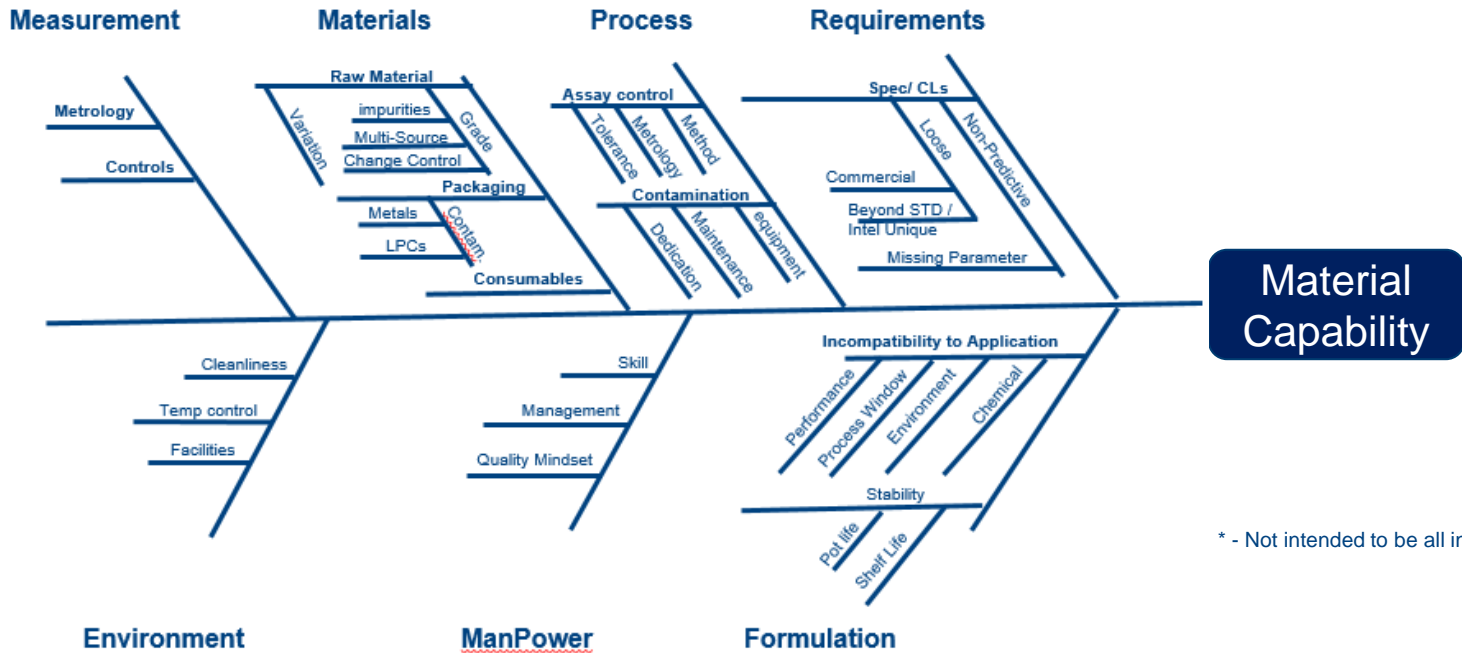
Train
sub-suppliers

Understand and
**segment
the supply chain**

Ensure
**business
continuity**

Follow the
EICC
Code of
Conduct

Material Performance Depends on Many Factors

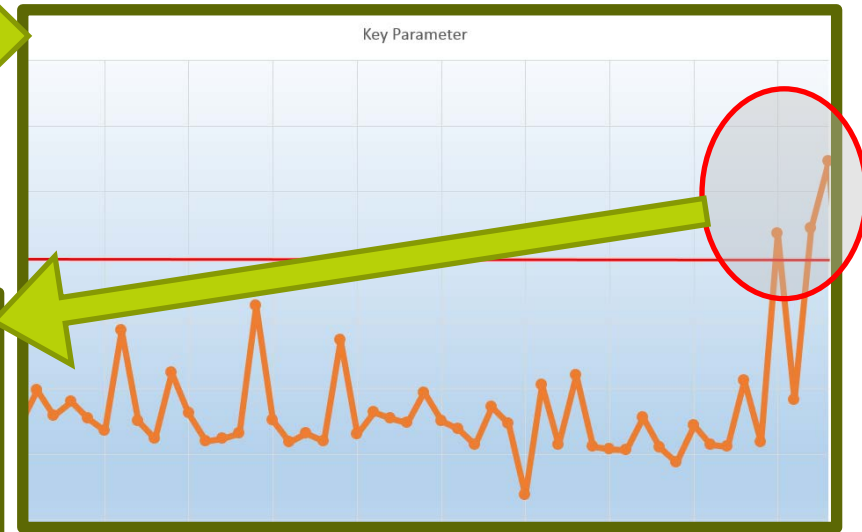
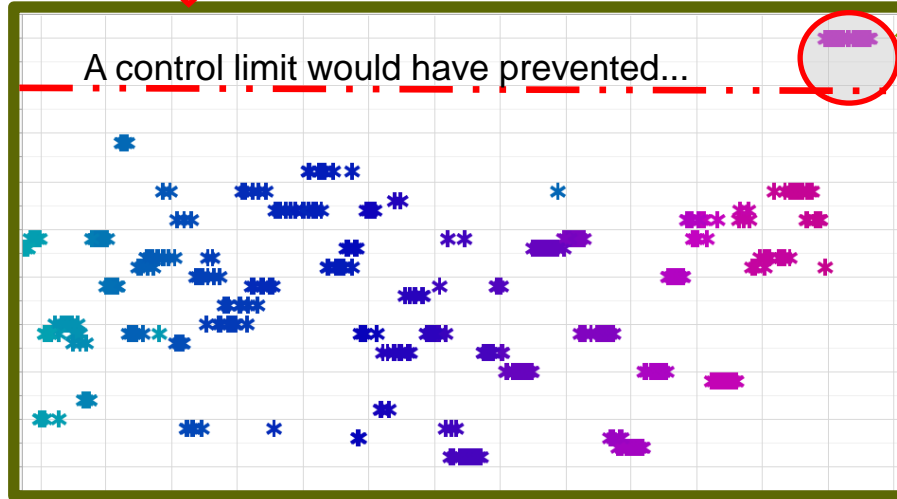


Deep **Supply Chain Understanding** is needed to Mitigate Risk

Process Control: Raw Material example

END RESULT:
Product level Spec Violation

Root Cause:
Lack of statistical scrutiny on RM

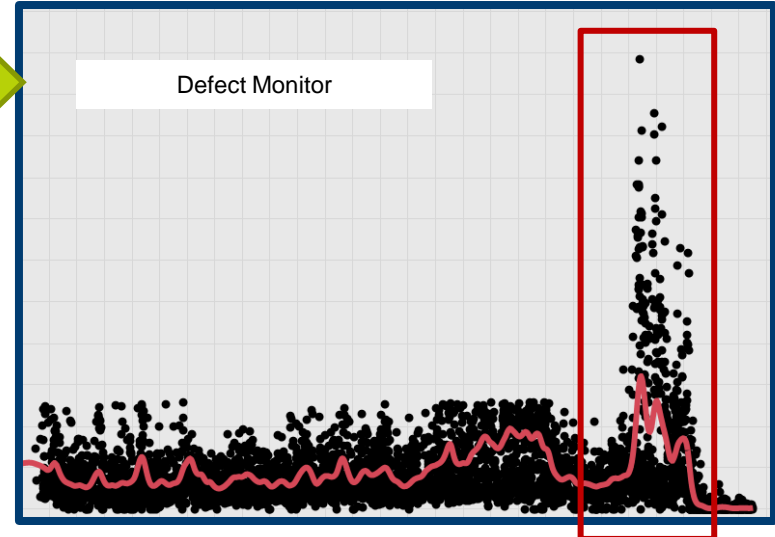
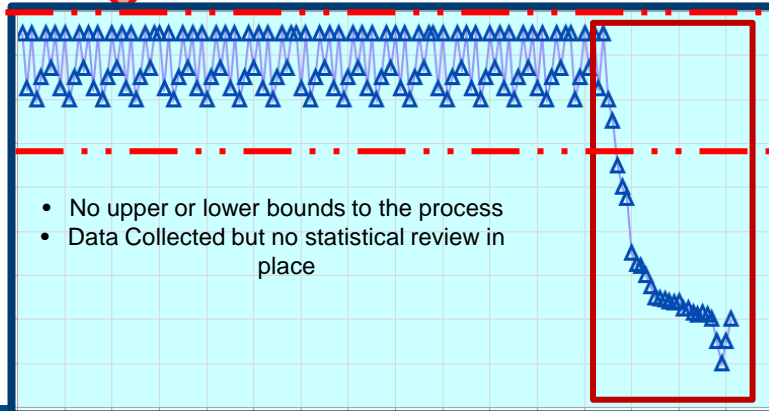


Control incoming materials with same
criteria
&
Respond to Outliers

Process Control: Inline metrics

END RESULT:
Inline Defect Issue at End-User

Root Cause:
Lack of statistical scrutiny in sub-supplier Process variables



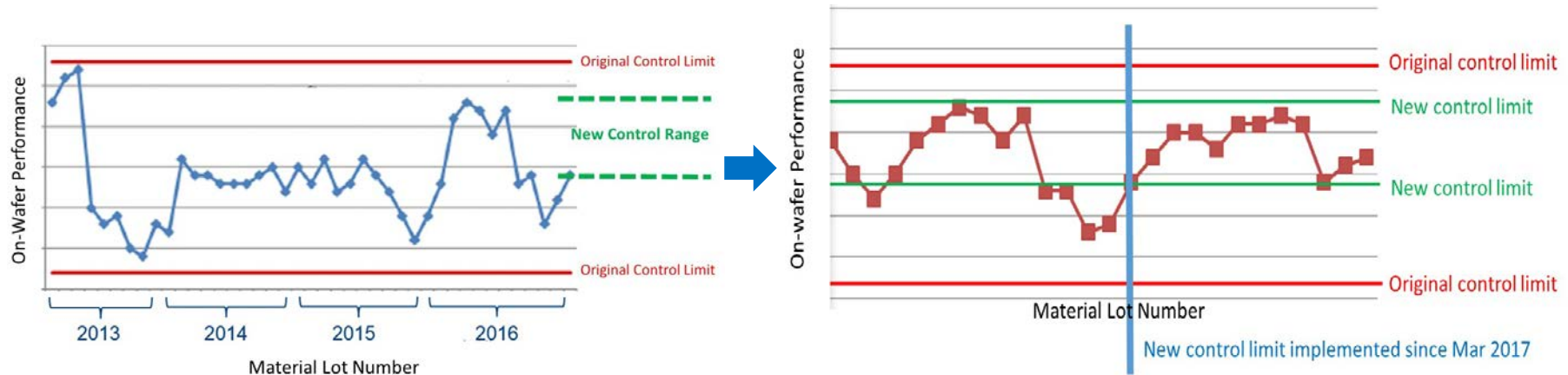
- Manage sub-supplier processes with the same 3 sigma criteria
- Respond to Outliers
- Lower is not always better
- Process variables should be bounded on both sides

Process Control: In the Supply Chain

Challenge: Process maturing at the customer generates **new material control requirements**.

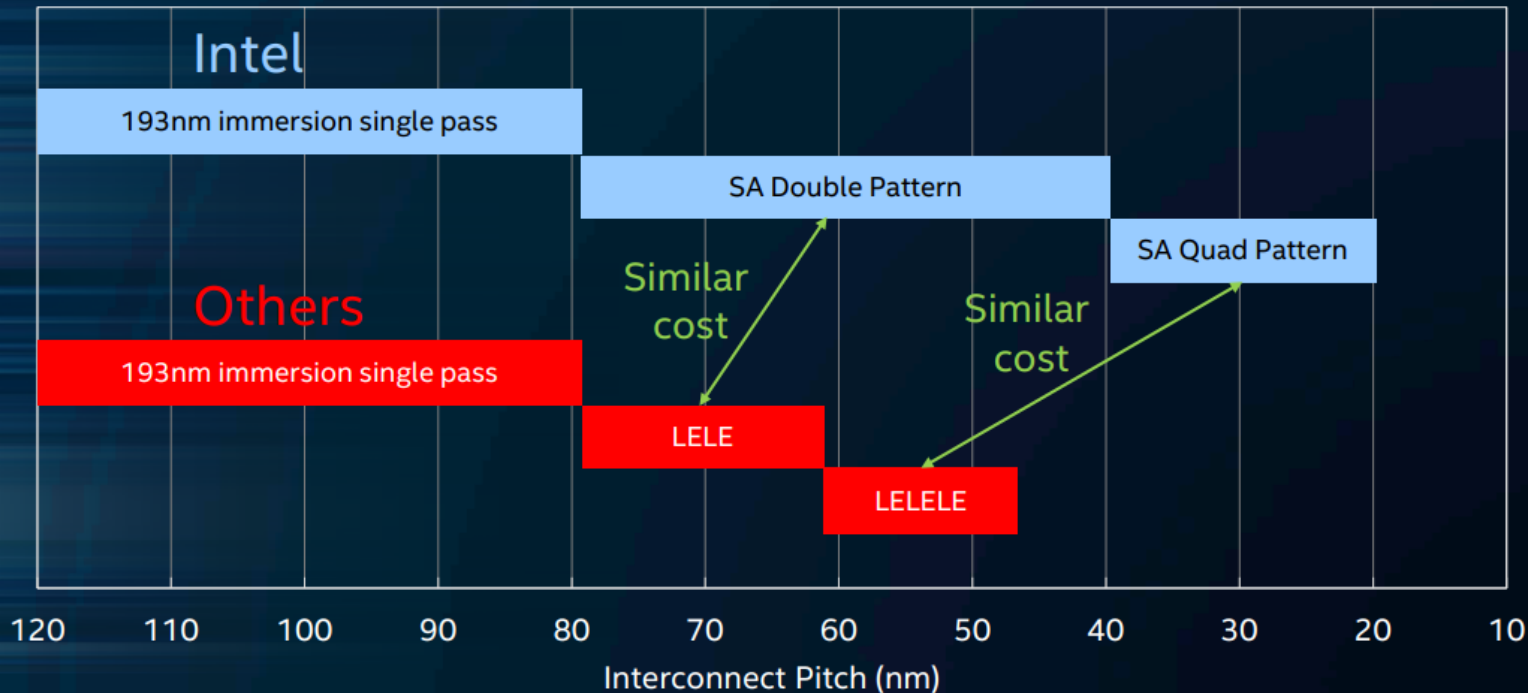
What worked in the past will not be sufficient in the future.

Solution: Determine **Raw Material Correlation** to On-Wafer Performance and **Tighten Process Control at Raw Material supplier**



Patterning Challenges for Advanced Logic and 3D-NAND

INTERCONNECT PATTERNING OPTIONS



Self-Aligned Patterning allows Intel to have dense interconnects at lower cost.

SELF-ALIGNED PATTERNING LEADS TO PROCESS CONTROL

Self-Aligned Double Patterning



Litho-Etch-Litho-Etch



LELE process has yield and performance risk with mis-alignment between patterns.

Emerging Patterning Technologies

EUV:

Extreme Ultraviolet

M-EBDW:

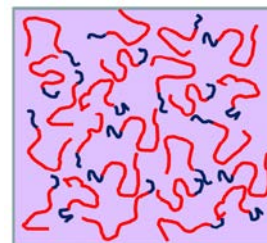
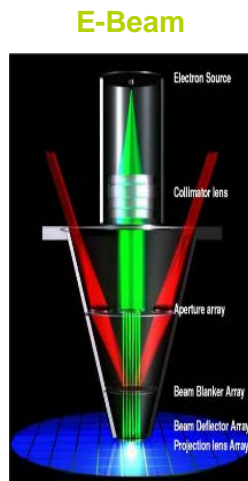
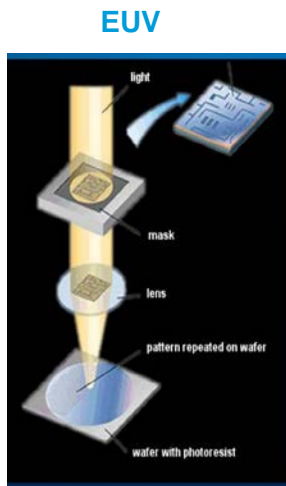
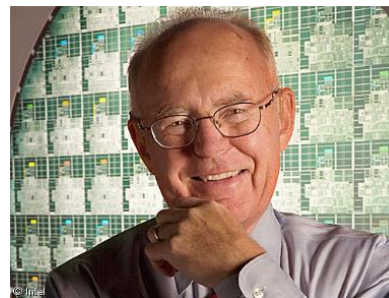
Multiple E-Beam Direct Write

DSA:

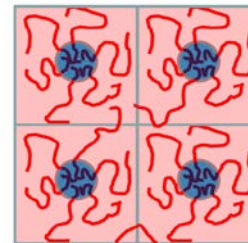
Directed Self Assembly

NIL:

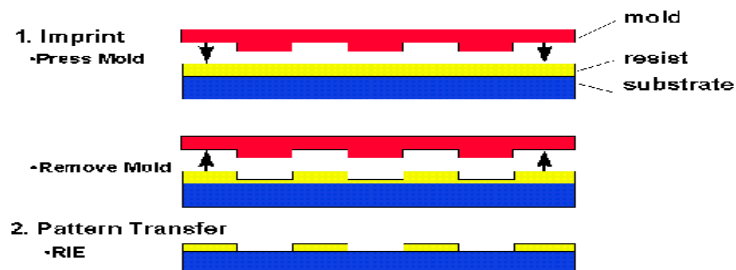
Nano Implant Lithography



annealing



DSA



NIL

New Technologies vs ArF Immersion

	Matl Defects	Matl Cost	Matl HVM	Tool Avail	Mask/ Mold	Through- put
EUV	Similar	Medium Risk	Similar	Medium Risk	High Risk	Medium Risk
M-EBDW	Similar	Medium Risk	Similar	High Risk	N/A	High Risk
DSA	High Risk	Medium Risk	Medium Risk	Similar	Similar	Medium Risk
NIL	High Risk	Similar	Similar	Medium Risk	High Risk	Medium Risk

 : Similar;  : Medium Risk  : High Risk  : N/A

ARF Immersion is still the **Main Workhorse** in the near future

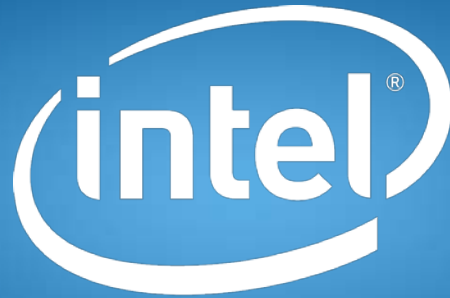
Summary

Entire semiconductor **Supply Chain** is working harder than ever to advance **Moore's Law**

Material **Capability** and **Consistency** requirements run **Deep** into the supply chain

Novel **Materials and Patterning** techniques bring **New Challenges**





experience
what's inside™