

IPMS

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Cobalt Fab Intro & Integration from CVD to CMP (R&D Accelerator)

L. Gerlich, M. Wislicenus, J. Koch, A. Dhavamani, S. Esmaeili, R. Krause, B. Uhlig

CMC Conference 2018

FRAUNHOFER INSTITUTE FOR PHOTONIC MICROSYSTEMS IPMS CENTER NANOELECTRONIC TECHNOLOGIES (CNT)

Königsbrücker Straße 178

01099 Dresden

Germany

www.ipms.fraunhofer.de

CMC Conference 2018 April 26-27, 2018 | Phoenix, AZ

Critical Materials for Device Driven Scaling



Outline

Cobalt Integration Solutions from the R&D Accelerator

- Introduction IPMS-CNT
- Motivation
- Cobalt
 - In BEoL Cu Metallization
 - Silicidation
 - TSV
 - Advanced Integration
- Conclusion





Fraunhofer Institute for Photonic Microsystems IPMS



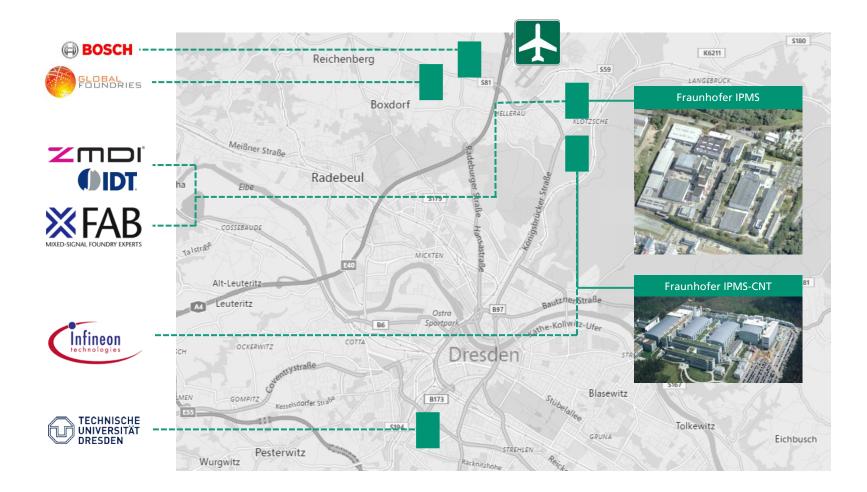








Fraunhofer IPMS Locations within "Silicon Saxony"







Overview



- 1500 m², class 10
- \rightarrow 200 mm (8") wafer line
- 3 shift preparation for R&D and pilot fabrication
- Technological parameter supervising system
- PPS based planning and documentation
- ISO 9001 certification



- >800 m² clean room, class 1000 &
 650 m² laboratory area
- >40 Tools for Wafer Processing, Patterning, Metrology & Analytics
- Qualification of processes & materials on
 300 mm industrial standard equipment
- Sub-nm characterization and verification
- Full integration into customer process flow in 28 nm technology and beyond

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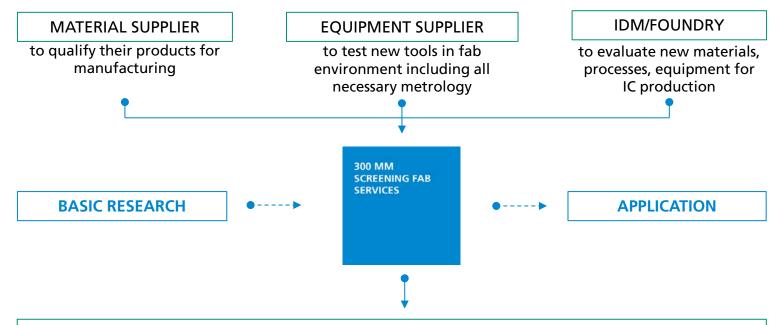
Cu metallization line @ IPMS-CNT

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ETCH	CLEAN	BLS	ECD	ANNEAL	СМР	FILMS	LITHO
AMAT	Semitool	AMAT	Semitool	TEL	AMAT	AMAT	Vistec
Centura	Raider SP	Endura	Raider ECD	Formula	Reflexion-LK	Producer	SB3050 DW
Dielectrics Metal HM open Ash	Front- /Backside Spray Megasonic Solvent	Cu PVD Ta/TaN PVD TiN PVD Co-CVD - Volta In-situ XPS	Cu ECD Co ECD	H2/N2	Cu Barrier Co Oxides STI	Oxides Nitrides Low-K ULK carbon	40 nm lines 30 nm holes p/n resists Spin-on processes









NEW MATERIALS, PROCESSES & INTEGRATION SCHEMES

- Consumable benchmarking
- Process enhancements and further cost reductions
- Next generation technology development
- Integration, optimization, qualification



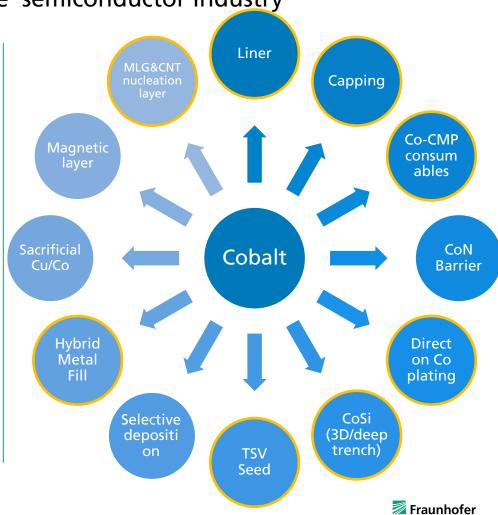




Motivation

Co MOCVD as a flexible process for the semiconductor Industry

- Some history of Co in CMOS
 - 250 nm node: CoSi2 introduction (PVD) (1990s)
 - **32 nm** node: CoWP introduction as capping layer (ELD)
 - **1x** nm node: Co-liner for copper metallization
- Challenge
 - Each technology needs normally a separate chamber
 - Usage one chamber (CoO)
 - Benefit from new properties





Cobalt

Cobalt as EHS sensitive material



- As a **metal**
 - After nickel and chromium, cobalt is a major cause of contact dermatitis
- Organometallic compounds (CVD/ALD precursors)



58.933

27

- Usually full encapsulated in Bubblers
- For maintenance/service still an issue \rightarrow high procedure standards

CCTBA (dicobalt	CpCo(CO) ₂		
hexacarbonyl t-	(Cyclopentadienyl		
butylacetylene	cobalt dicarbonyl)		
$H_{3}C$ $H_{3}C$ C C C C C C C C C			

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Cobalt

- Organometallic compounds (CVD/ALD precursors)
 - Usually full encapsulated in Bubblers
 - For maintenance/service still an issue \rightarrow high procedure standards
- Cobalt electrolytes CoCl₂, CoSO₄ for **Plating**
 - It is crucial to avoid crystallization to fulfill EHS requirement
 - Gender selectivity to work directly with the electrolyte is recommended

Key message: EHS is relevant, but right procedures avoid blocking points!



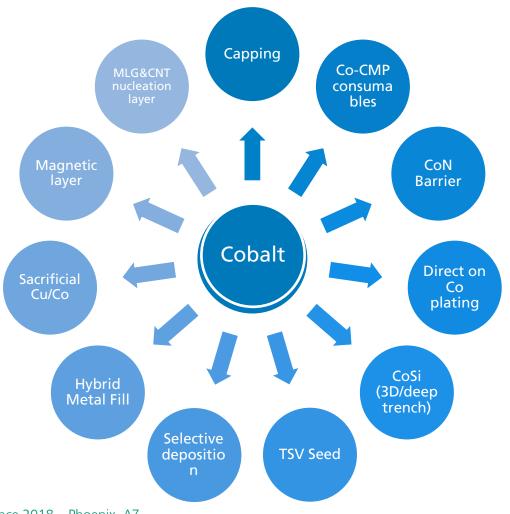














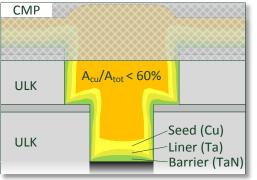


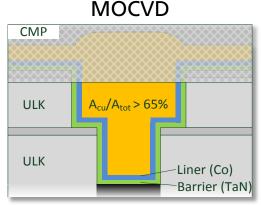


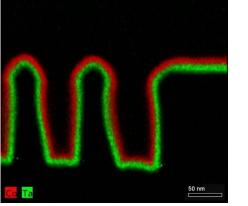
Cobalt in Copper Metallization

Integration of Liner

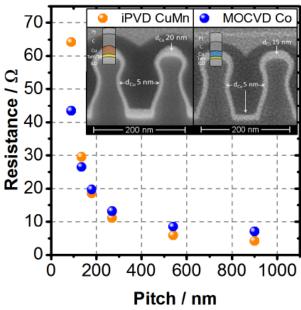
- Requirements
 - Low resistivity
 - Pin hole free
 - As thin as possible
- For usage as liner below Cuseed <2 nm Co is recommended</p>
- Strict controlled conformity with CCTBA as MOCVD-precursor PVD







EDX/TEM : Conformal deposition in small structures (28 nm node)



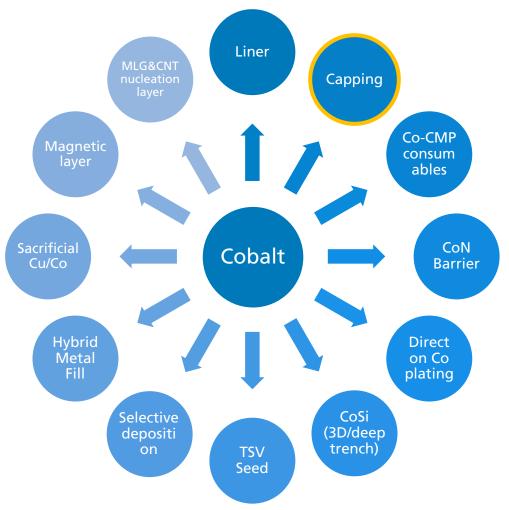
M.Wislicenus et al. MAM 2018



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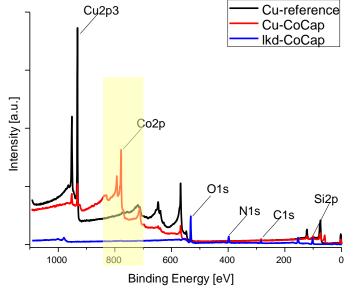


Cobalt as capping

- Benefits
 - EM stability/reliability
 - Route compatibility
 - Low CoO \rightarrow combination of Co

Process	Сар	ССТВА	CpCo(CO) ₂	
	Pressure	5 torr	20 torr	
	Temperature	100°C	≥200°C	
	flow	200 sccm	< 50 sccm	

- Area selective deposition shown
 - CpCo(CO)₂ as superior capping material
 - CCTBA selective for a narrow thickness range <1nm



XPS of CpCo(CO)2 capped lkd and Cu wafers (+Cu ref)





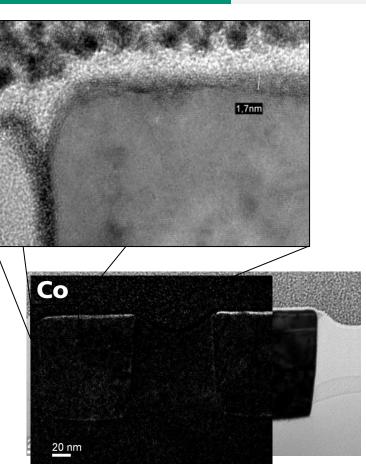
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Cobalt as capping

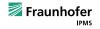
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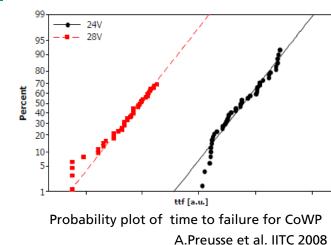
(EF)TEM of Cu-lines after selective Co-MOCVD capping with CoCp(CO)2

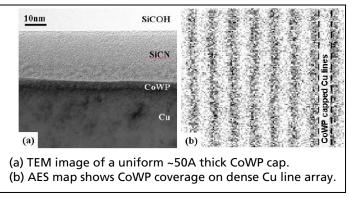




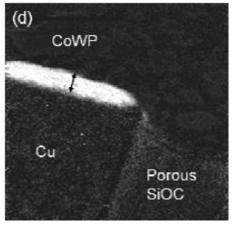
CoWP as capping

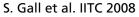
- Electroless deposition was introduced by AMD for the 32 nm node in production in 2009
- Superior reliability data were achieved
- Difficult to operate
- CoWP eless chemistry was monitored for EHS

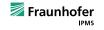




A.Preusse et al. IITC 2008



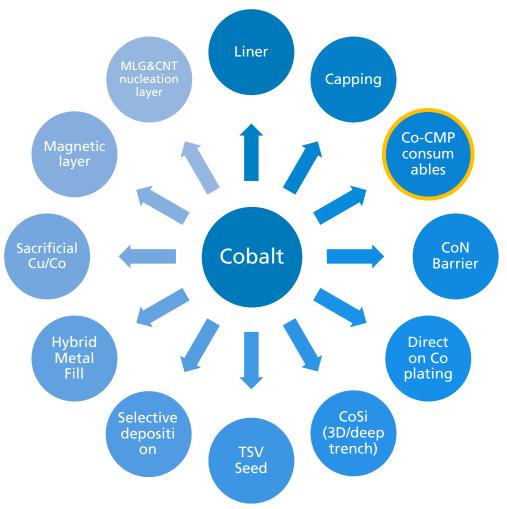




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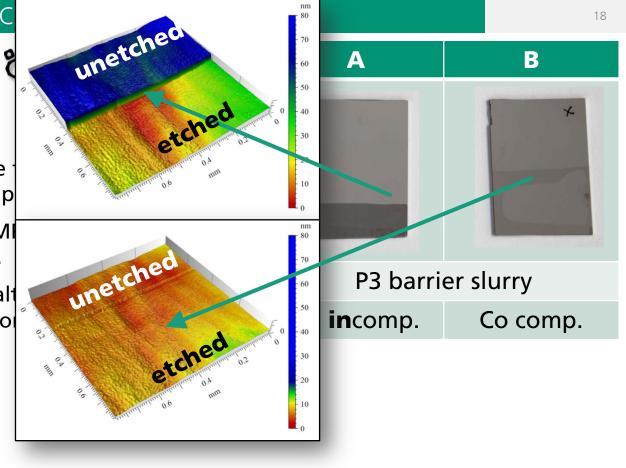


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Cobalt-**CMP** consumables

- Co is very sensitive therefore to CMP p
- Slurry and post CMI be Co compatible.
- CMP of filled cobalt in investigation (cor







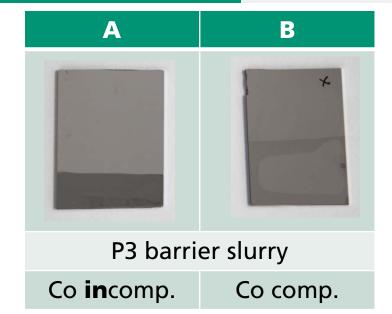
Cobalt in Copper Metallization

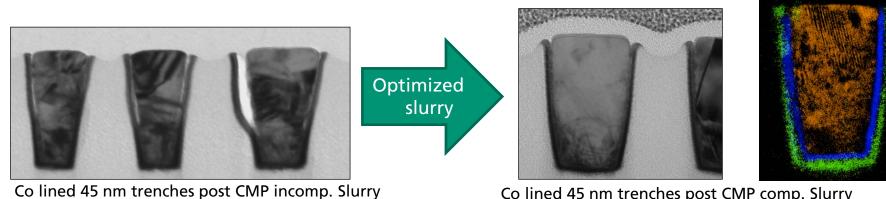


Cobalt-**CMP** consumables



- Co is very sensitive to corrosion and therefore to CMP processes.
- Slurry and post CMP clean have to be Co compatible.
- CMP of filled cobalt lines still in investigation (consumable screening)





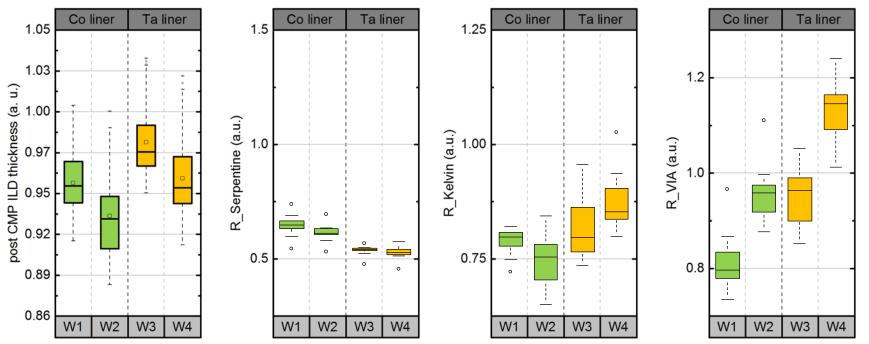
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Co lined 45 nm trenches post CMP comp. Slurry J. Koch et al. ICPT 2015



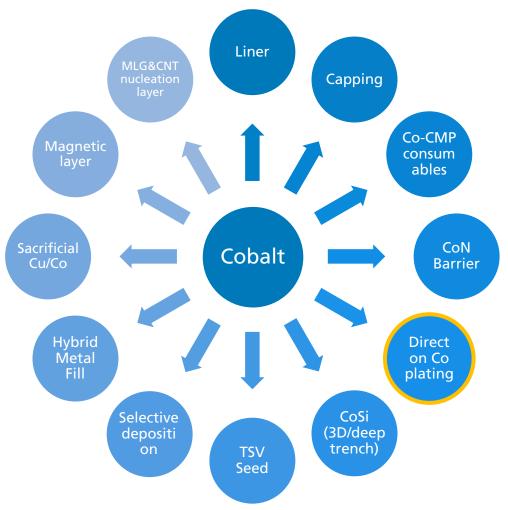
Cobalt-CMP - Integration of Co liner for CMP tests

Co liner Ta liner



Enhanced electrical performance up to 30 % of 28-nm-node interconnects using Co as liner material.
J. Koch et al. ICPT 2015



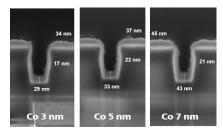


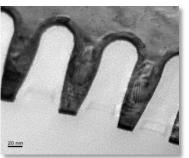




Direct on Cobalt plating

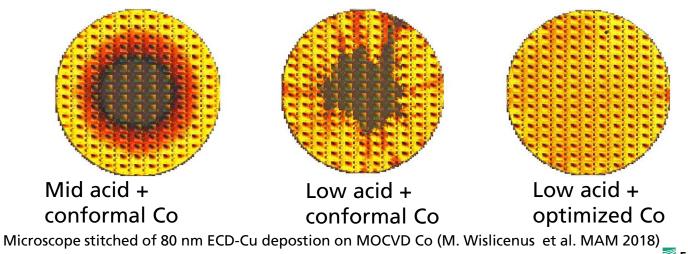
- Direct plating of Cu on Co
 - Certain thickness and dep. mode allows direct plating on Co seed





TEM of Cu plt in narrowed structures

- Electrolyte/seed conductivity ratio affects the fill performance
 - Less feature effects at high bath and low seed conductivity
 - Strong feature effects at low bath and low seed conductivity

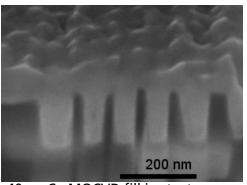




Cobalt fill approaches on cobalt seed

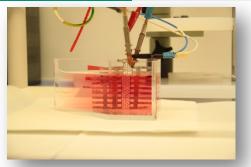
Co MOCVD

- 😕 Slow
- 8 Carbon contamination
- 😊 Flexible
- Reflow option
- Prefill option

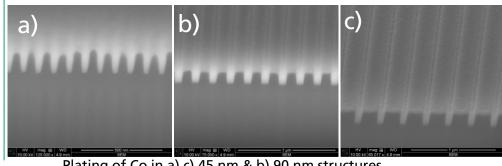


40nm Co MOCVD fill in stuctures

- Co **ECD**
 - 🙂 Fast



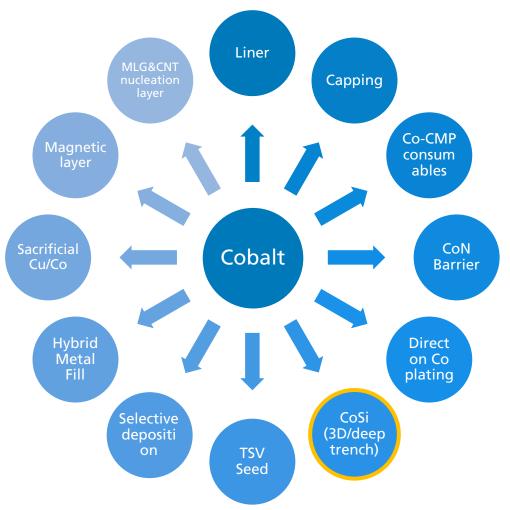
- Seamless fill & reflow
- Eimited to additive functionality
- 8 EHS concerns but possible
 - Scale up to 300 mm tool



Plating of Co in a),c) 45 nm & b) 90 nm structures





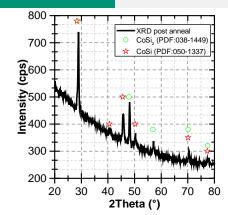




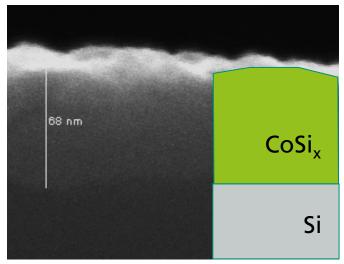


Co- silicidation

- Co silicide formation well known as gate silicide via PVD
- Co MOCVD meets future requirements of 3d integration
- Process
 - CCTBA direct on HF-treated Si
 - <10 torr (low pressure)</p>
 - 150°C deposition
 - CoSi formation by RTP annealing in N₂
- Possible carbon contamination could be an issue but basic feasibility is shown



XRD of Co-MOCVD layers on Si show after anneal processes the formation of CoSix.



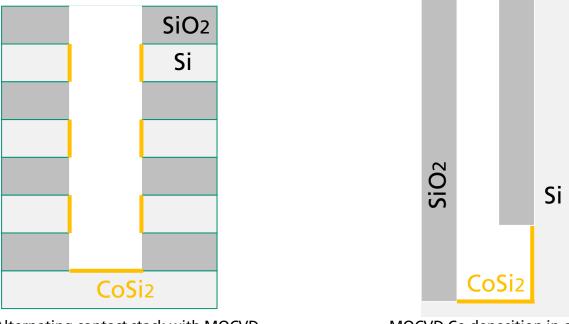
X-SEM of 20 nm Co after anneal for silicidation

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Co- silicidation

- Cobalt silicide formation well known as gate silicide via PVD
- Co MOCVD meets future requirements of 3d integration

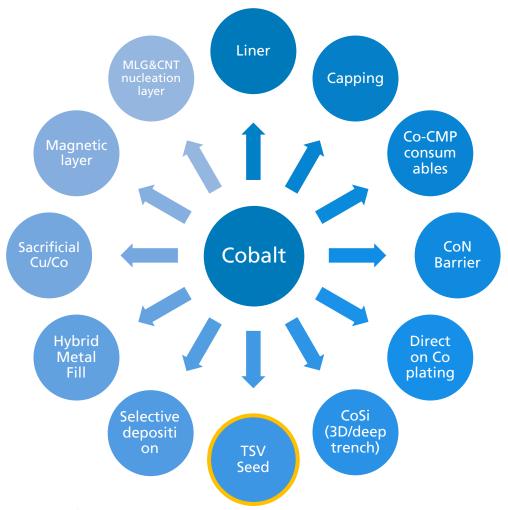


Alternating contact stack with MOCVD Co deposition and silicidation

MOCVD Co deposition in cavity and silicidation









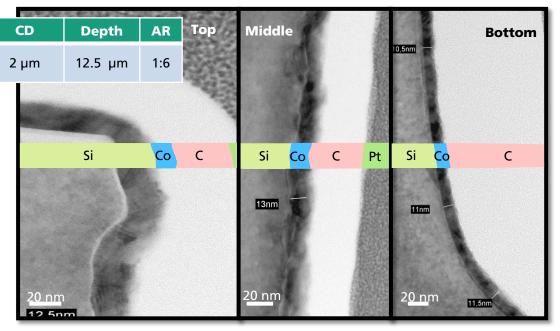
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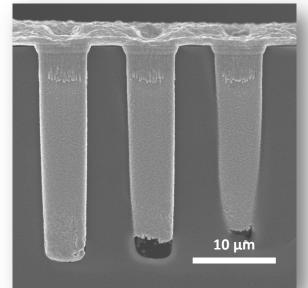


TSV Seed

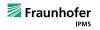
Co Thin Films as an Alternative Seed Layer for **TSV** Metallization

- Co liner for high aspect ratio TSVs
- Direct plating with Cu

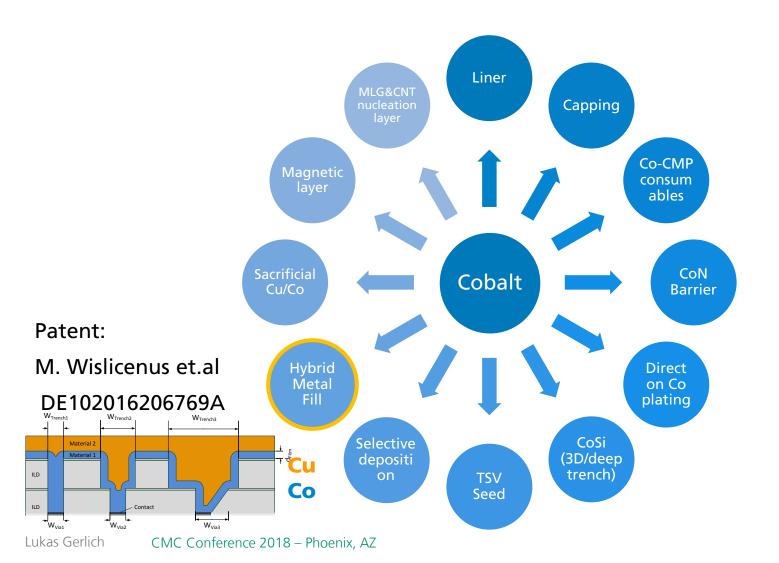




- Cu deposition without additives
- Conformal deposition possible

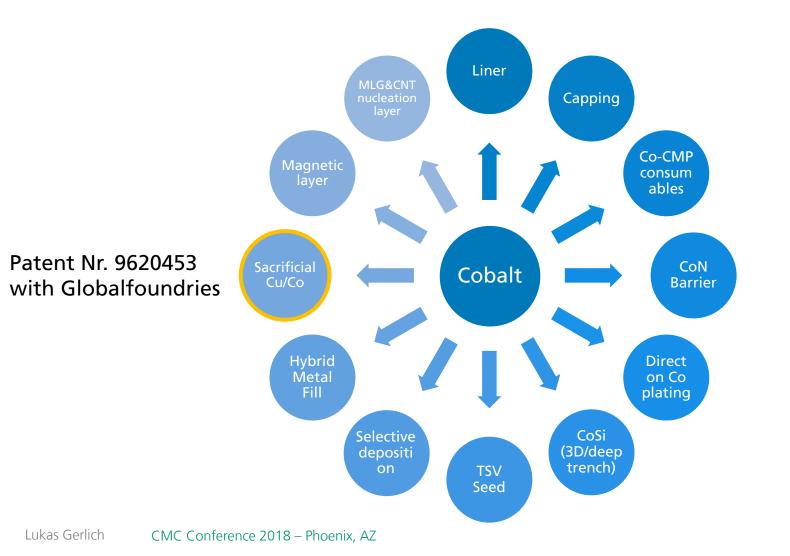






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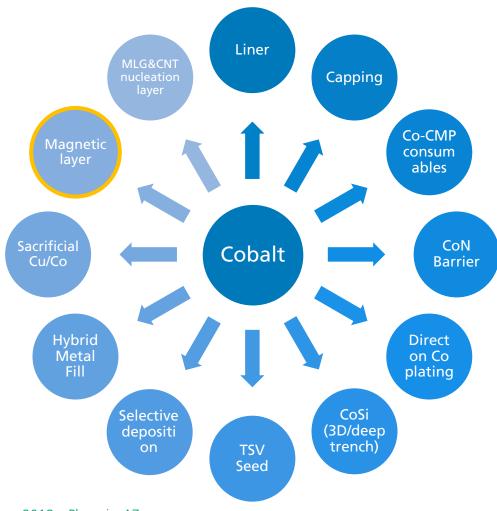


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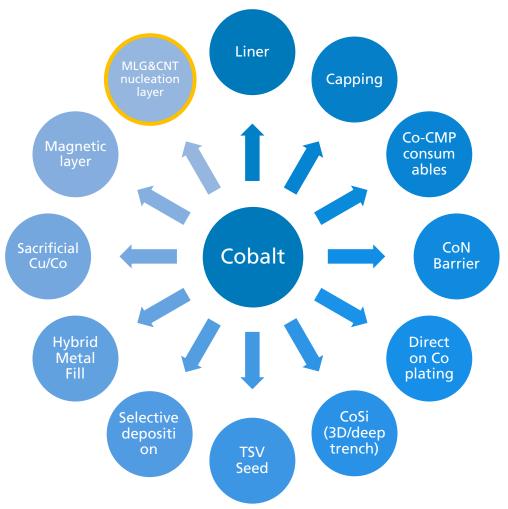


- Multi target cluster PVD tool for NVM in purchase
- ECD formed pillars in investigation









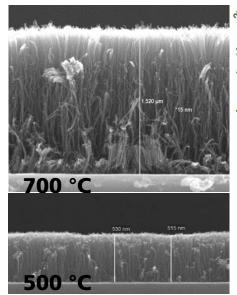


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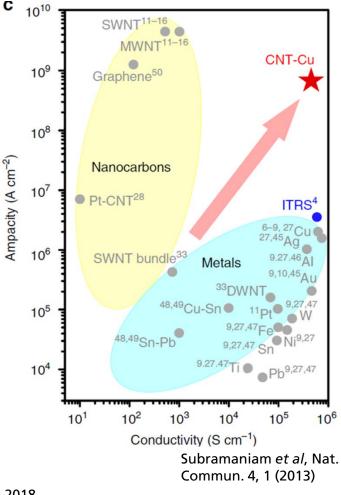
Cobalt as CMOS compatible catalyst for CNT growth c

- CNT-Cu composites with good conductivity (performance) and high ampacity (reliability) are desired
- Challenge:
 - CMOS compatibility
 - Manufacturability
- Cooperation in EU Project with Aixtron for **300 mm** wafer processing



CNT growth on Co catalyst for different temperatures

B. Uhlig et al., Date 2018



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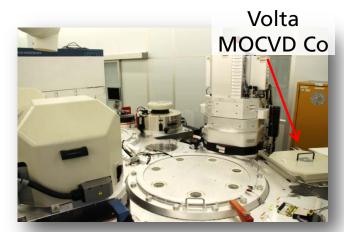


Cobalt Deposition **MOCVD** tool

- AMAT Endura II 300 mm + Volta chamber with dual bubbler system
- Bubbler are ready to install \rightarrow safe procedure
- EHS issues are solvable
- Flexible for different applications

Cobalt Deposition **ECD** tool

- Semitool Raider ECD 300 mm + DoB chamber
- Electrolytes with EHS sensitive issues
 - Strict procedure for usage; clean tool policy
 - Transfer & storage has to be monitored
- EHS issue can be managed



AMAT Endura II system at Fraunhofer CNT



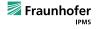
Semitool Raider system at Fraunhofer CNT

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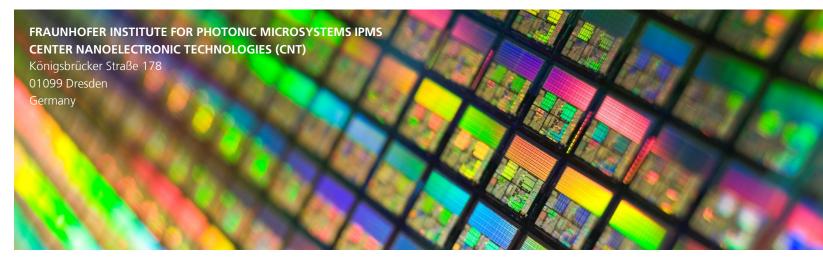
Conclusion

- Cobalt as promising material will be used in semiconductor fabs in future and has proven to be usable
 - in a industrial compatible process flow
 - as a competitive material
- Further advantages of a MOCVD-process (sidewall coverage, cavity reach) may be utilized for example
 - for 3d integration
- Cobalt ECD as very promising technique for contact level and local interconnects filling and magnetic applications are under invetigation





Thank you for your attention!



www.ipms.fraunhofer.de | www.cnt.fraunhofer.de | www.screening-fab.com

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