Silicon Wafer Quality at GLOBALFOUNDRIES

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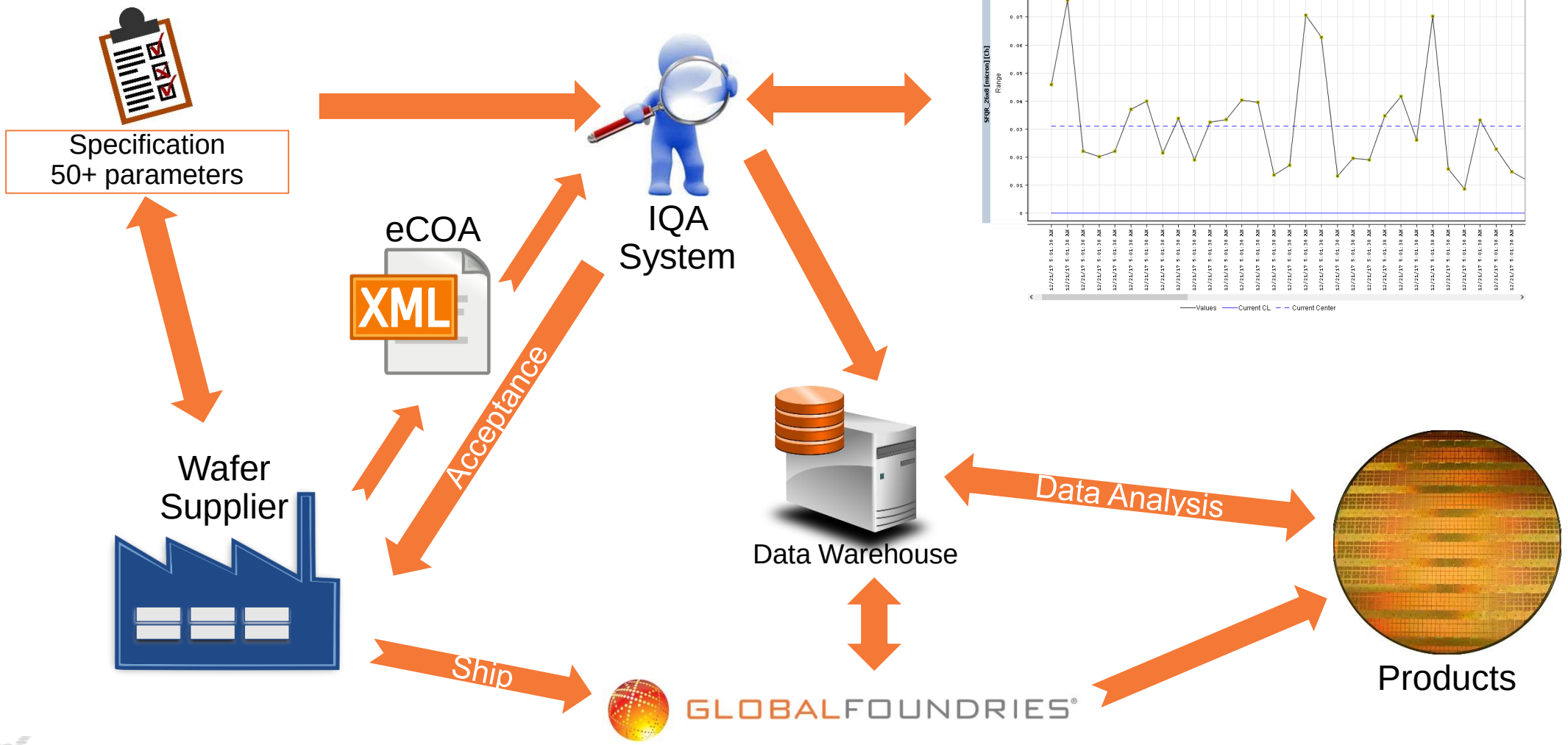
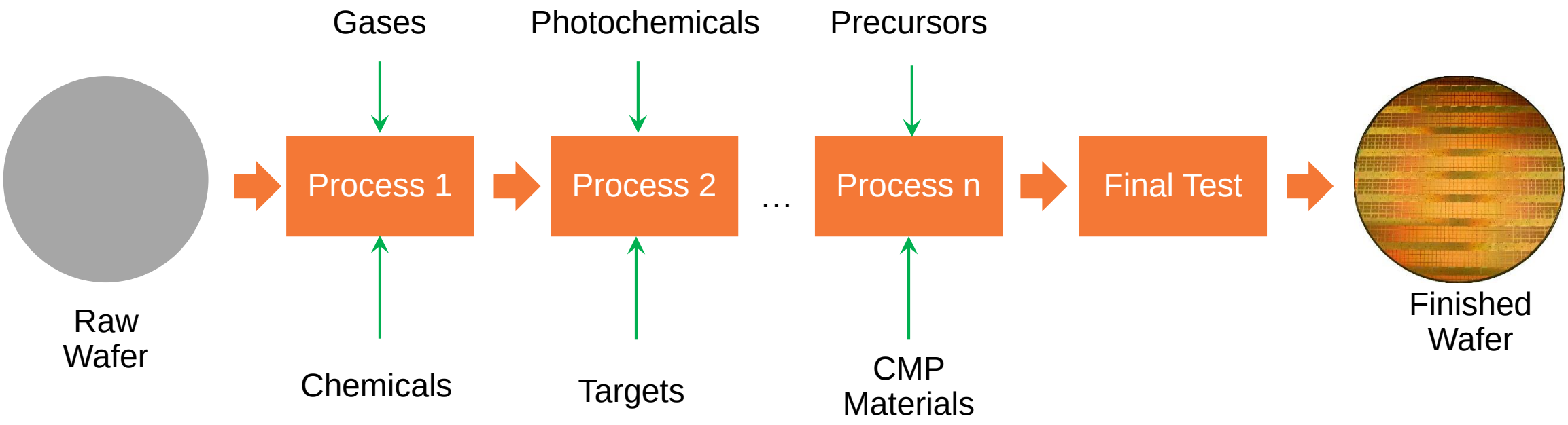
Overview

- Incoming Quality System
  - Specifications
  - Incoming Quality Assurance System (IQA)
- Supplier Mismatches & Interactions
  - Metal Pattern Defects
- Metrology Challenges & Limitations
  - New failure modes on advanced technologies (humps)
  - Site level data (Wafersight, SPx, etc.)
- Future Opportunities

Incoming Quality Overview



Many Opportunities to Affect Wafer Quality/Yield



n > 700 process steps for advanced node process!

Specification

- Typical parameters, methods, defined by SEMI standards.
  - Thickness, flatness, defects, resistivity, etc.
  - Typically single value (mean, maximum, minimum)
- Incoming data has FOSB (Front Opening Shipping Box) ID and wafer level reporting. This information is mapped to the MES for wafer start.
- All FOSBs have RFID and registered at wafer start.
- Sorter does an exact match on physical wafer ID and wafer IDs in the MES on lot start.
- Data is linked to the wafer throughout the life cycle.

IQA System

- Generates XML template from specification
- Accepts eCOA data from suppliers
  - Generally wafer-level data for 300mm
- Compares to:
  - Specification
  - SPC Control Limits
- Transmits acceptance to supplier
  - Approval to ship
- Ensures that no OOS/OOC wafers reach GF Site
- eCOA data is available to the Data Warehouse/Yield Analysis System
  - Correlation to parametrics, yield, defects

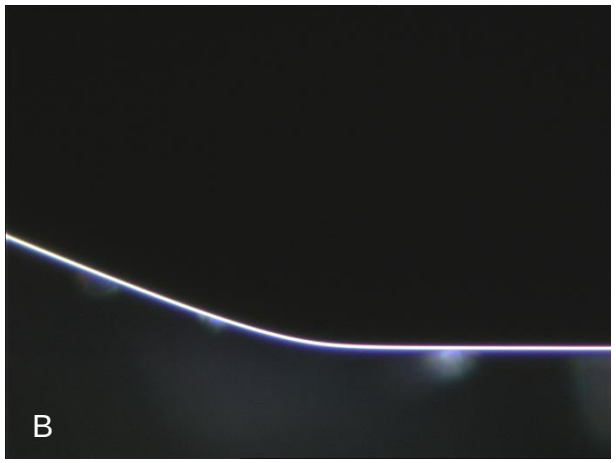
But...

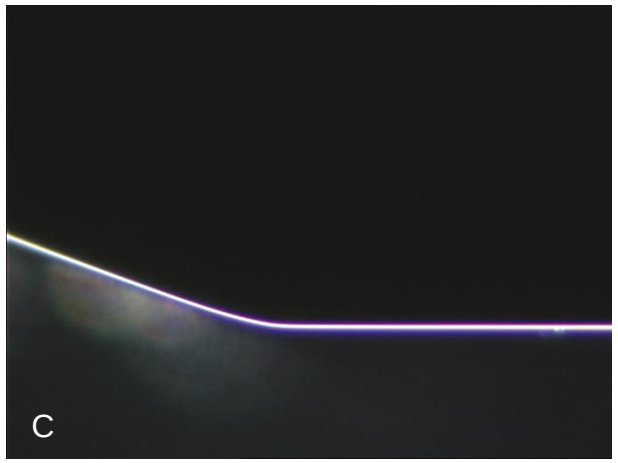
We usually don’t have problems with specified parameters!

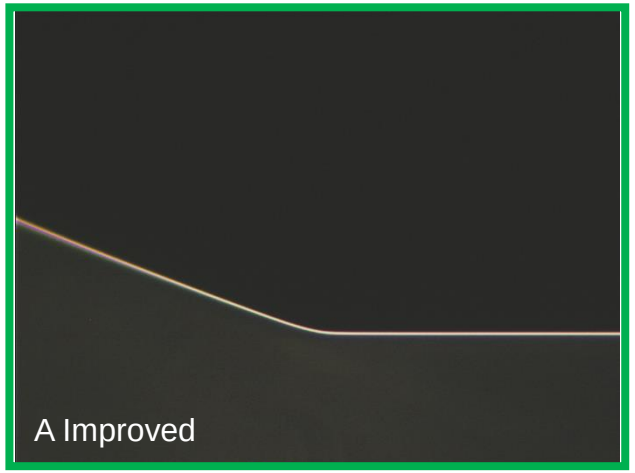
Potential Problems

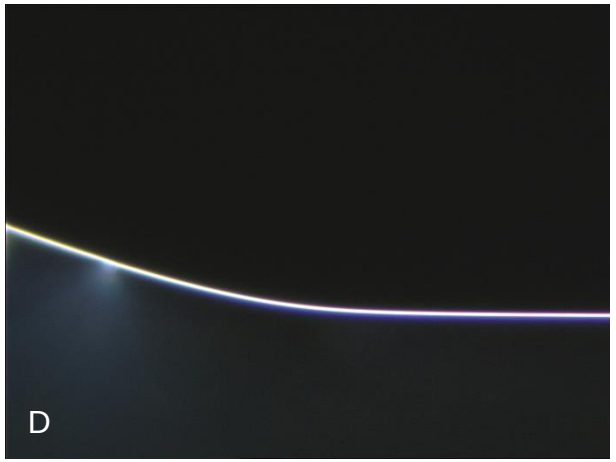
- Unspecified Parameters
  - Ex. Edge profile, “humps”
- Metrology Capability
  - Ex. Defects below bare wafer threshold
- Interactions with other variables
- IT Infrastructure Capability
  - Ability to accept wafer maps, instead of values

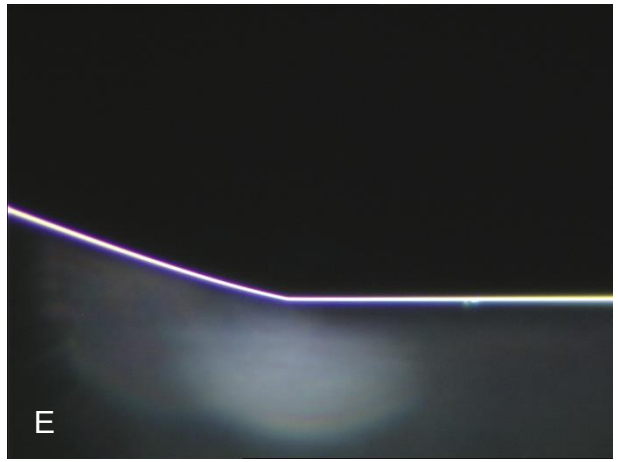
Backside bevel shape

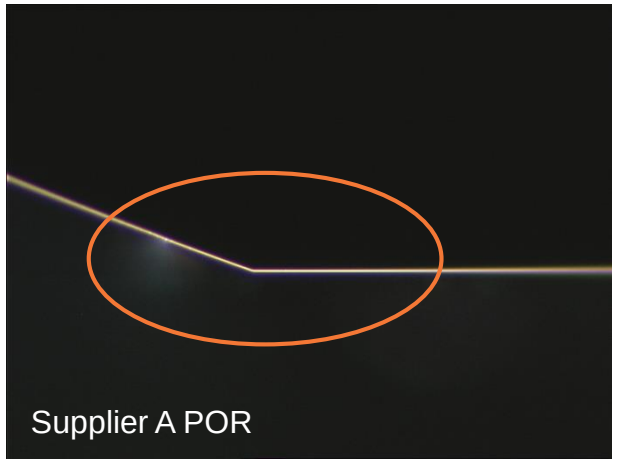








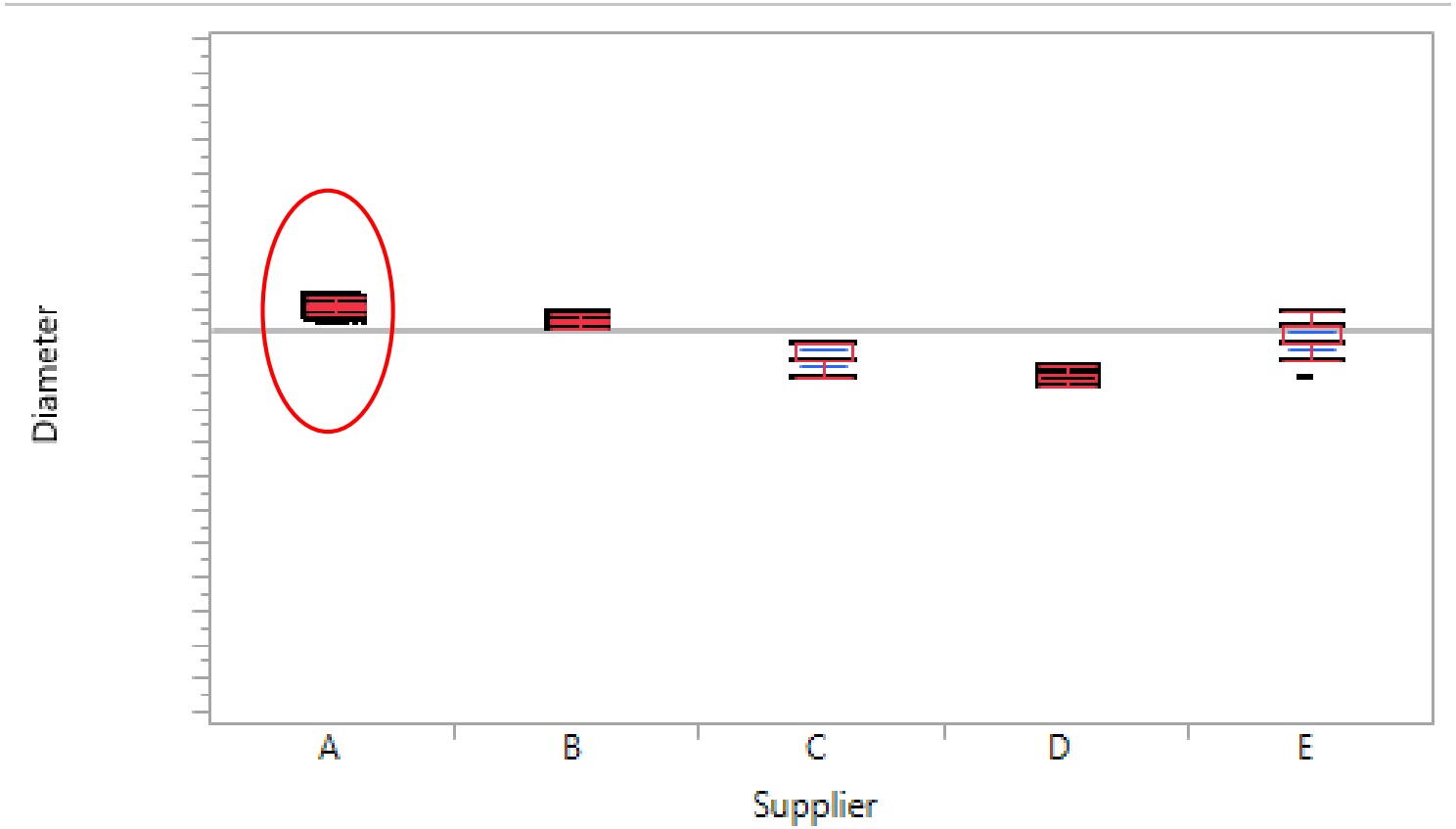




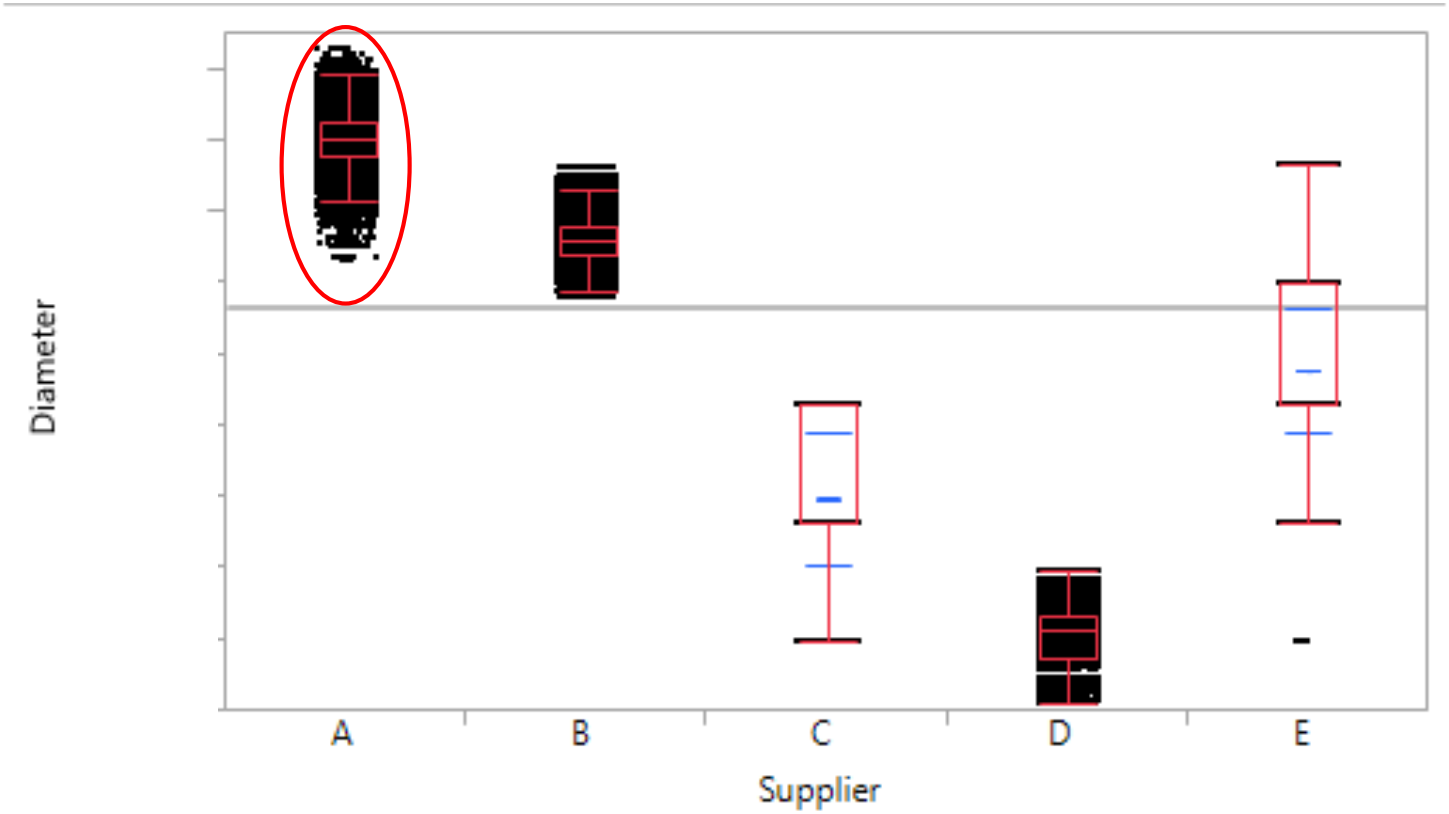
- Supplier A show clear kink
- D shows smoothest edge
- Supplier A Improved shows smoother edge than POR.

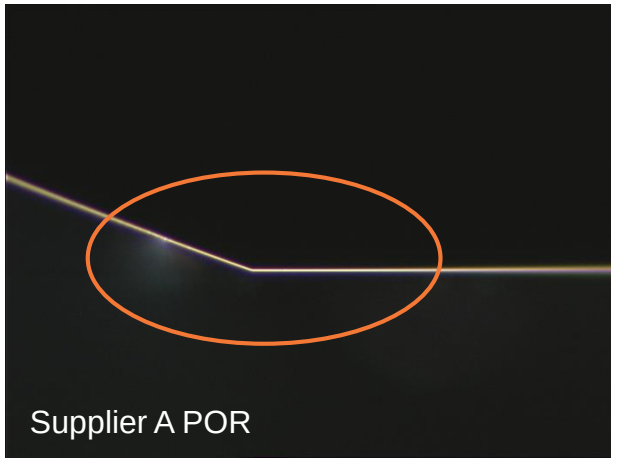
By: Pascal Limbecker

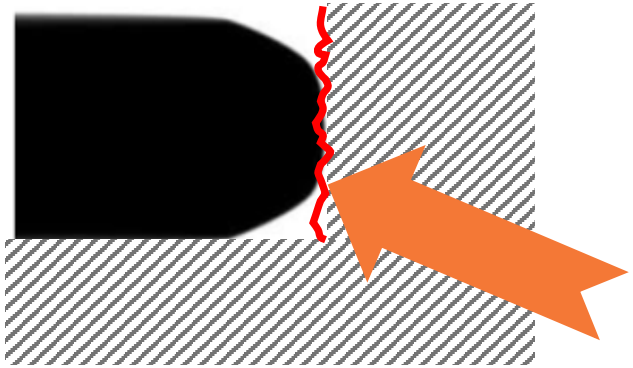
Diameter



Diameter





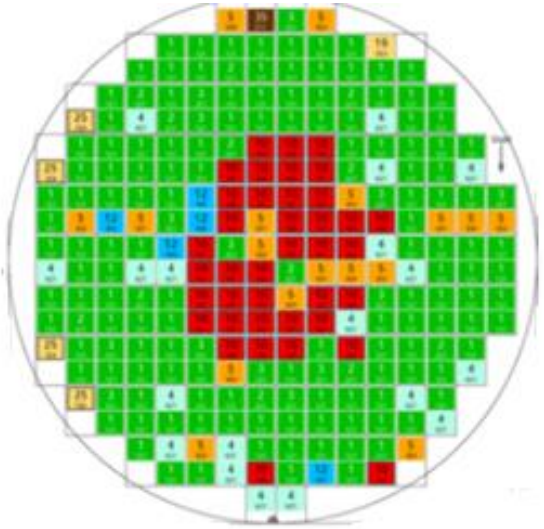


Conclusion: Small difference in diameter combined with the sharp kink on the edge profile contributed to the high defectivity.

Incoming Wafer Defects - Humps

Observation

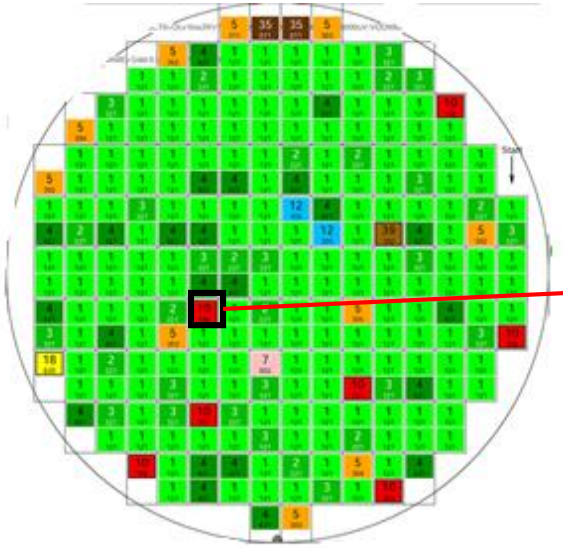
- Starting from an observed SORT center spot signature. Failure analysis revealed defects on the incoming Si.
  - All low yielding wafers are processed on a double side polish machine with a reduced slurry flow
  - Standard defect detection (SPx LPD) does not detect these defects.
- FA shows humps of about 300µm width an up to 120nm height (observed)

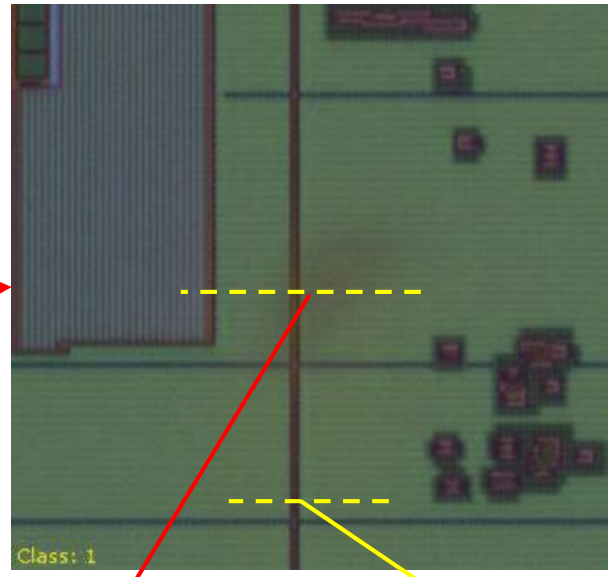


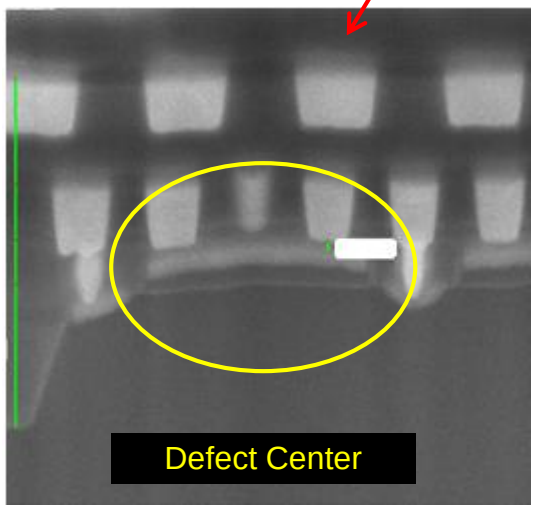
Impact

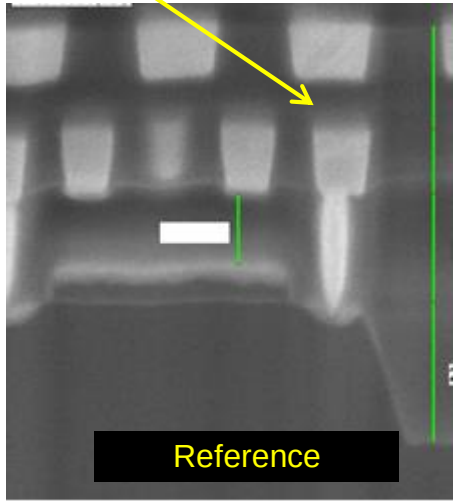
- Failure modes
  - Shallow trenches in the area of the defect
  - PC to M1 shorts in the area of the defects
  - No impact on > 40nm nodes

Humps – Failure Analysis

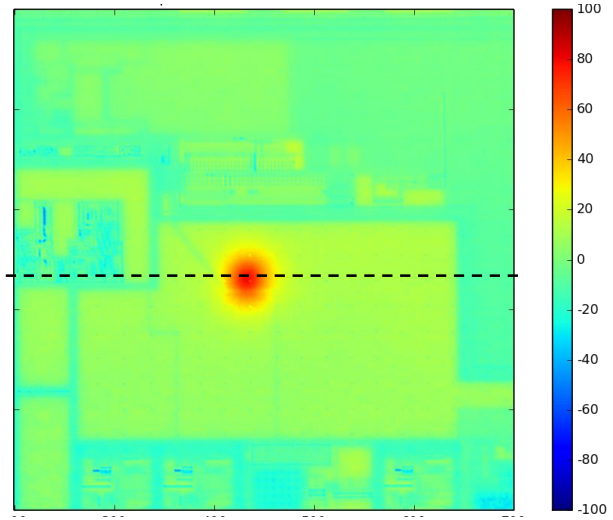


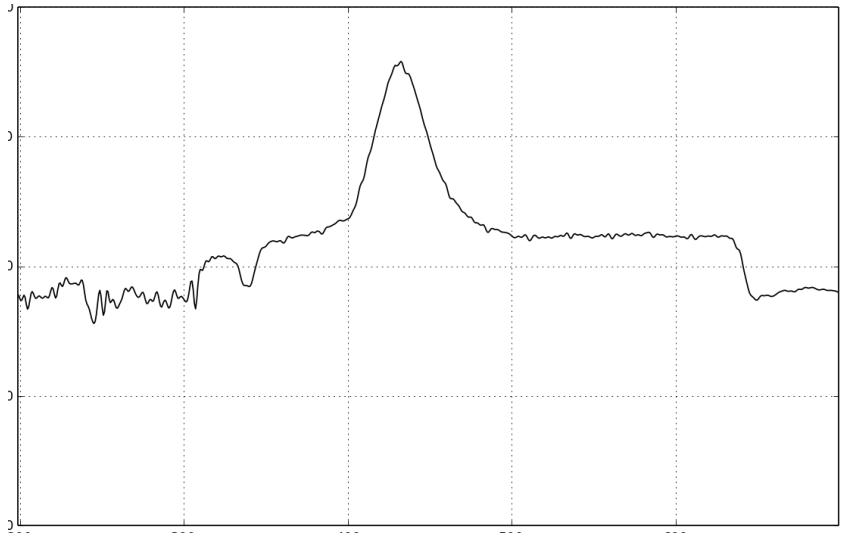


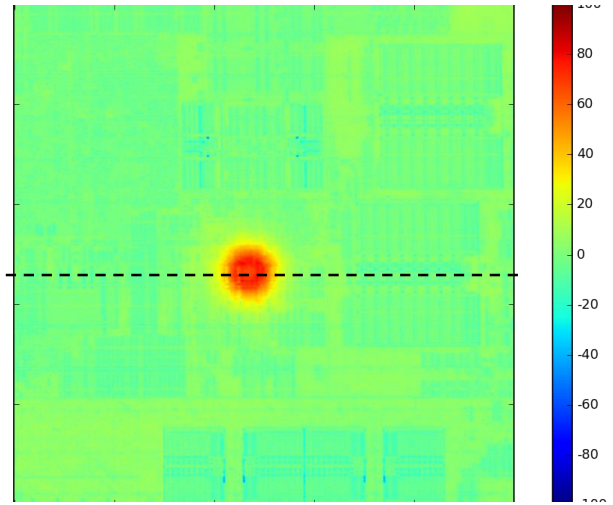


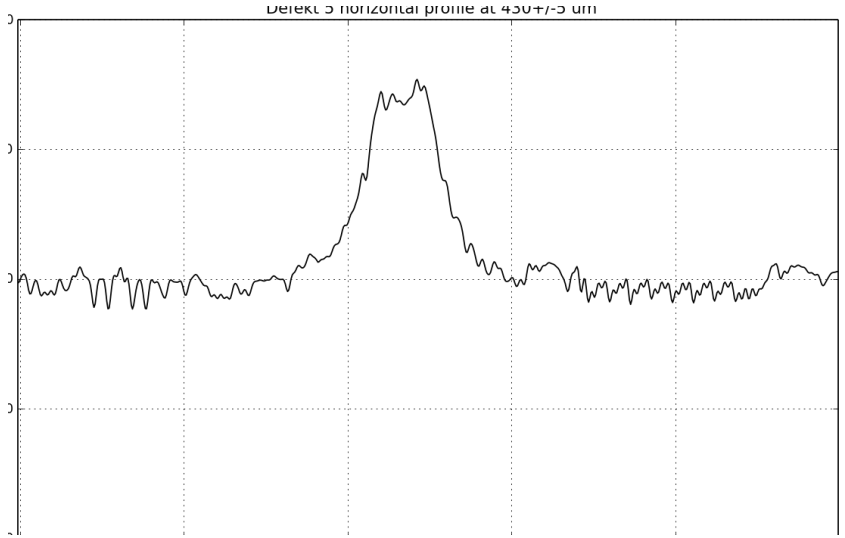


Humps - Failure Analysis



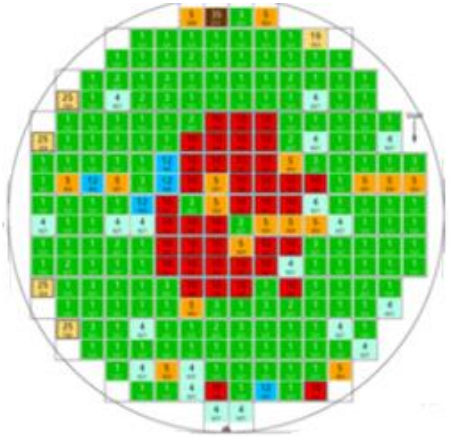


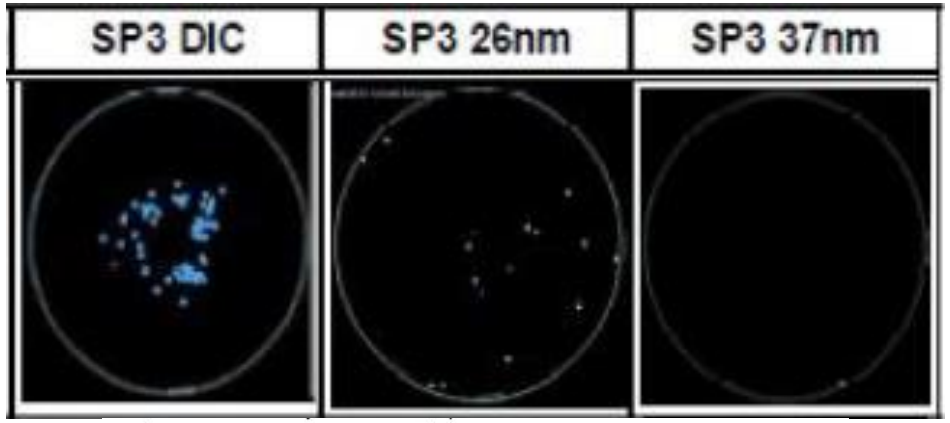


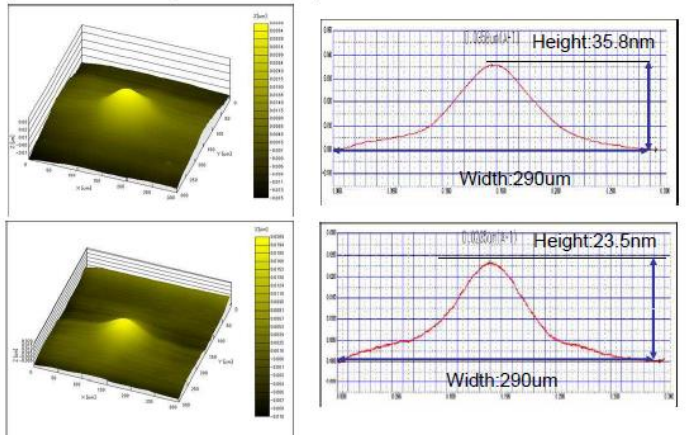


Humps

- Low aspect ratio of defects makes them invisible to LPD (Light Point Defect) channels on KLAT SPx.
- SPx using DIC (brightfield – differential interference contrast) mode is capable of detecting such defects
- Required establishing baseline for all suppliers, and adding an additional parameter to spec

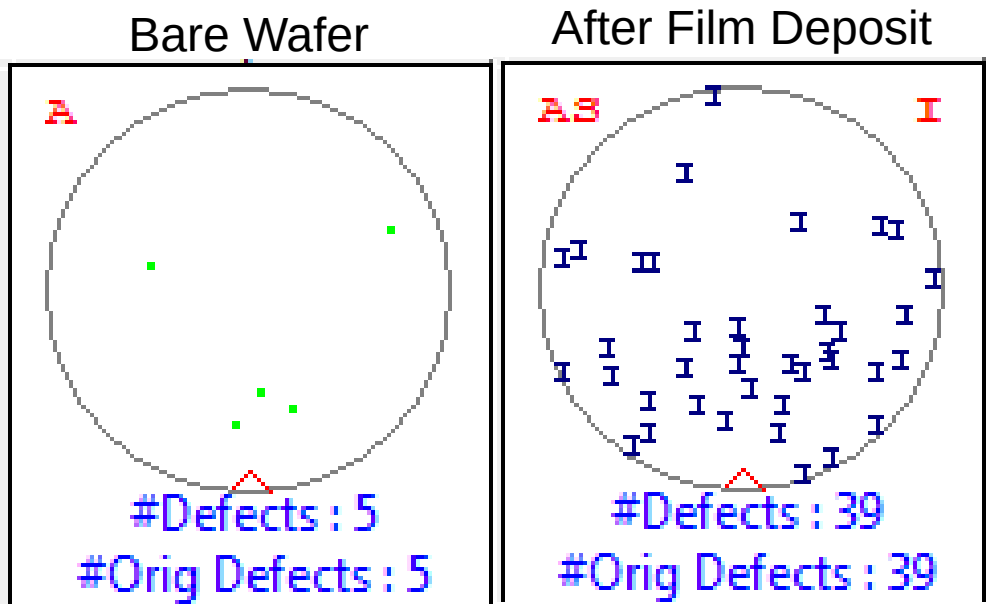


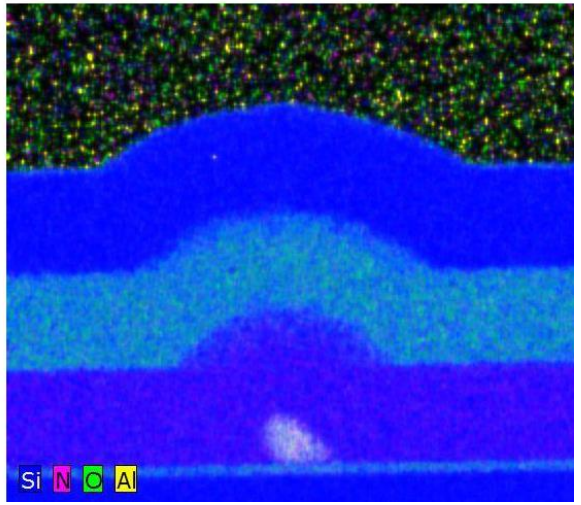




Subthreshold Particles

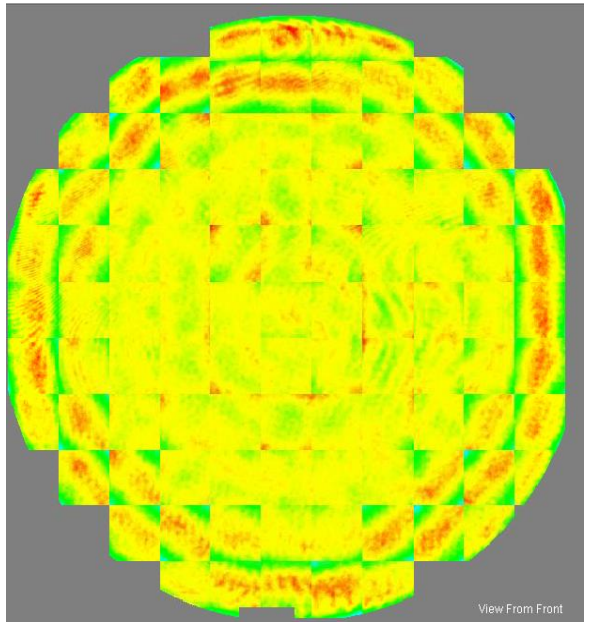
- Scenario
  - Wafers pass particle limits spec
  - Wafers pass incoming inspection
  - Wafers processed through thin film deposition
  - Wafers fail for particles
  - Tools investigated for problems, test runs
- Root cause is often very small particles
- Need better detection capability on bare wafers!

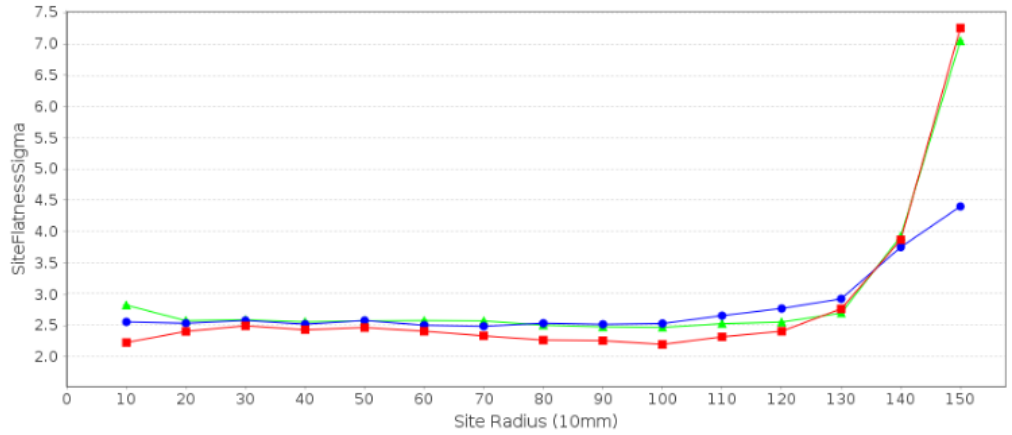




SFQR Maps (Wafersight)

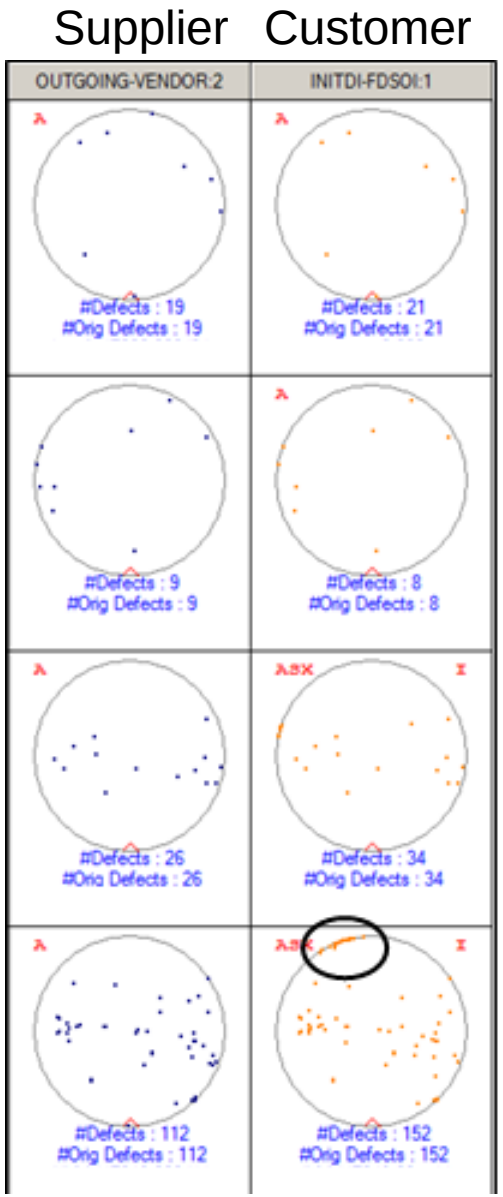
- Site Flatness TIR
  (Total Indicator Reading)
- Variation across wafer makes wafer-level correlations poor
- Would be helpful to have site level data for importing to the Yield Analysis System
  - Enables die-level correlations to geometrical parameters
  - Use existing KLARF file format



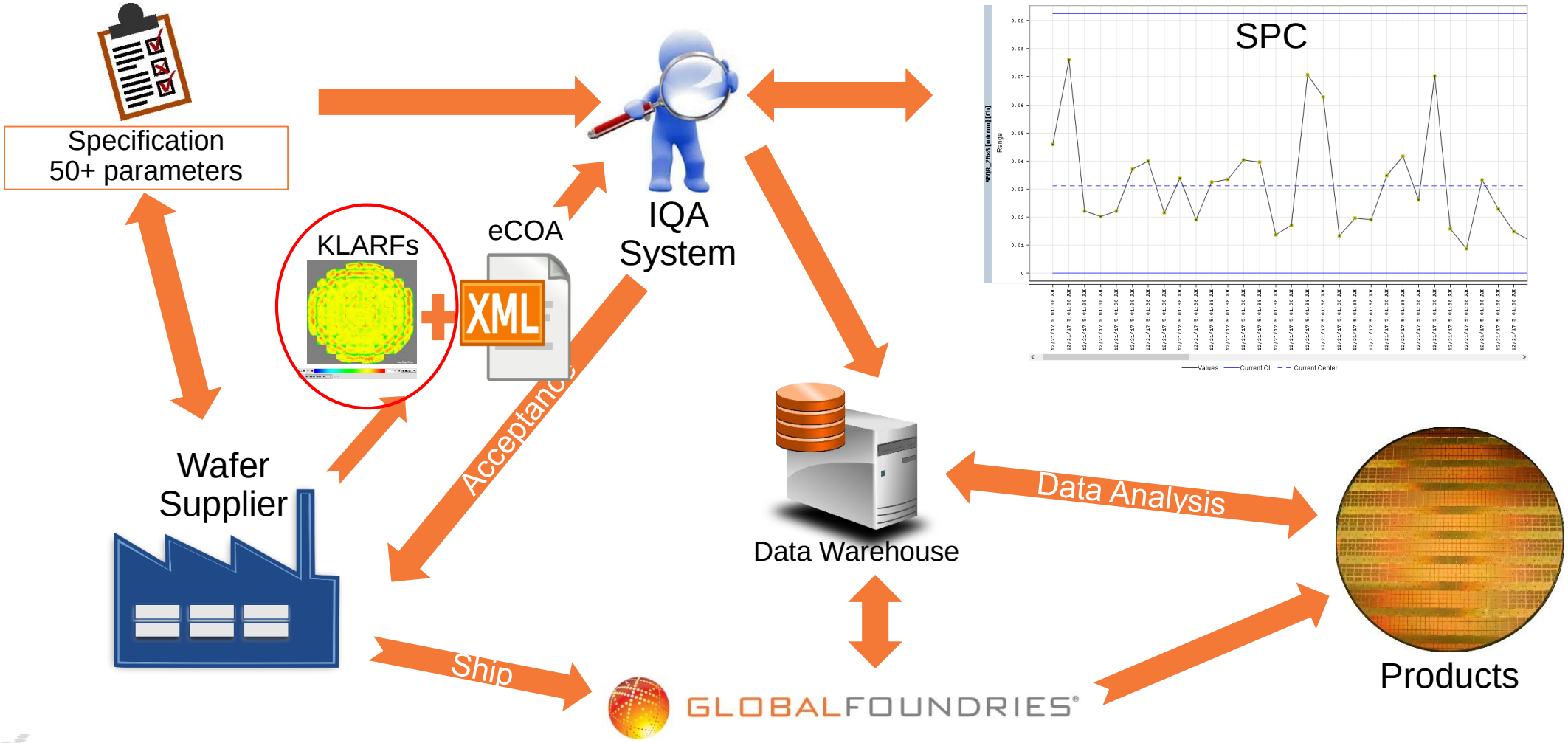


Defect Maps

- Suppliers measure 100% of wafers on Defect Inspection Tools
- We get summary parameters like Total Defect Count, etc.
- But, the map data is not transmitted
  - Defect coordinates, size, classification
- Would be preferred to have wafer maps (KLARF files) for import into Yield Analysis System
  - Compare defect maps incoming (customer) vs. outgoing (supplier)
  - Better detection of transportation/wafer unpacking problems



Opportunities for Improvement



Summary

- New failure modes driving addition of additional parameters
  - > 50 parameters on advanced epi wafers
  - More on SOI
  - Many yield-impacting defects visible only with newer metrology
- Many parameters are spatially non-uniform
  - Require wafer maps to correlate to device yields/performance
- IT Infrastructure to support massive amounts of data transfer from wafer suppliers really does not exist
  - Has been done on limited basis, for limited number of lots
  - Not yet available on routine basis

Acknowledgements

- Jutta Auerhammer – Global Materials Engineering, Dresden
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Thank you!

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