



Semiconductor Materials Information

2015-16

TECHCET's Critical Materials Report on Advanced Insulating Dielectric Precursors

Prepared by

Ralph Butler

Reviewed by Jonas Sundqvist, Ph.D.

Edited by Lita Shon-Roy

Techcet CA LLC
PO Box 3056
Rancho Santa Fe, CA 92067

www.techcet.com

info@techcet.com

[+1-480-382-8336](tel:+14803828336)

RESEARCH METHODOLOGY

Techcet employs subject matter experts having first-hand experience within the industries which they analyze. Most of Techcet's analysts have over 25 years of direct and relevant experience in their field. Our analysts survey the commercial and technical staff of IC manufacturers and their suppliers, and conduct extensive research of literature and commerce statistics to ascertain the current and future market environment and global supply risks. Combining this data with Techcet's proprietary, quantitative wafer forecast results in a viable long-term market forecast for a variety of process materials.

Readers Note: This report represents the interpretation and analysis of information generally available to the public or released by responsible agencies or individuals. Data was obtained from sources considered reliable. However, accuracy or completeness is not guaranteed.

Table of Contents

1 Executive Summary	6
1.1 Supply Chain Challenges	6
1.2 Market Landscape	8
2 SCOPE	10
3 Dielectric applications Roadmap and Implications	10
3.1 Logic Transistor Evolution	12
3.2 Memory Evolution	16
3.3 Implication of Device Evolution to IC Fabs, Processes and Materials	20
3.4 Looking Beyond 2019.....	22
3.5 450 mm Wafers.....	26
3.6 Semiconductor Process Materials Supply Chain Trends	26
3.7 China's Influence on WW Materials Supply	27
3.8 Process Materials Volume Growth.....	27
3.9 Forecast of Wafer Starts by Nodes and Product Mixes by Year.....	28
4 Technical Challenges for Dielectrics Films	30
4.1 Dielectrics and 3D NAND	30
4.2 Interconnect Trends.....	30
4.3 Low K Dielectric : Copper Interface	33
4.4 Further RC Delay Challenges.....	33
5 Dielectrics Materials and Precursors	36
5.1 Lower K Dielectrics.....	37
5.1.1 FSGs (Fluoro-silicate Glasses) and CDOs (Carbon Doped Oxides)	39
5.1.2 SODs (Spin On Dielectrics).....	39
5.1.3 Porous Low K	40
5.1.4 Capping Layers and Barrier Dielectrics.....	42
5.2 Hardmasks and Diffusion Barriers	44
5.3 STI GAP FILL	45
5.4 SIDEWALL SPACER	49
5.5 PMD	52
5.6 R&D Considerations for CVD / ALD precursors	53
5.6.1 The CVD process.....	53
5.6.2 Considerations for spin-on precursors	56
5.6.3 Multi-Patterning	57
5.6.4 SADP – self aligned double patterning	58
5.7 Organic and inorganic precursors and related equipment set	60
5.8 ALD SiO₂.....	63
6 MARKET LANDSCAPE	65
6.1 Supply Value Chain Issues and Trends.....	68
6.2 Supply Base in Korea.....	71

6.3	Market Size/Forecast	73
6.4	Low Temp SiN Issues	76
6.5	Supplier Ranking by Application.....	77
7	Precursor Delivery	78
8	Future Outlook for Dielectric Precursors	81
9	Suppliers and Makers Profiles	82
9.1	Air Products Chemical Inc.	82
9.2	Air Liquide, USA	83
9.3	Nova-Kem.....	84
9.4	SAFC Hitech	84
9.5	UP Chemical Co., Ltd.	85
9.6	Gelest	86
9.7	TCI Chemicals.....	86
9.8	FujiFilm.....	87
9.9	Dow Corning	87
9.10	Praxair.....	88
9.11	Techno Semichem also known as SoulBrain	89
9.12	DNF.....	89

List of Figures

	page #
Figure 1: Dielectric Precursor Market Size Forecast (\$USD).....	8
Figure 2: CMOS Logic Device Transition	12
Figure 3: C ₃ D TriGate/FinFET	13
Figure 4: Comparison of Planar and 3D (TriGate/FinFET) CMOS Transistor. (A) Planar, (B)FinFET on Bulk Si& (C) FinFET SOI.....	14
Figure 5: One Version of InGaAS on Si wafer	15
Figure 6: MPU/MCU Device Roadmap May 2014.....	16
Figure 7: Schematic cross section of SK-Hynix HBM module. (Source: AMD HBM brochure, TechInsights)	17
Figure 8: Non-Volatile Memory Device Roadmap May 2014.....	18
Figure 9: Intel and Micron unique material compounds and a cross point architecture for a NVM memory technology (Source: Intel & Micron).....	19
Figure 10: 22nm FinFET Metal Gate Electrode Materials (ref. Chipworks ASMC 2014).....	21
Figure 11: Time Line Logic Device Technology through 202011.....	23
Figure 12: Forecast Silicon Shipment Trends by Node and Product Type (millions of 200mm equivalent wafers/year)	29

Figure 13: Low k Generation timeline	40
Figure 14: Pore Size Distribution Challenges (illustrated)	41
Figure 15: 2013 ITRS for Interconnect.....	43
Figure 16: Shallow Trench Isolation after densification.....	48
Figure 17: Profile of shallow trench isolation after HDP	49
Figure 18: Sidewall spacer formation	50
Figure 19: Sidewall spacer lateral offsets.....	50
Figure 20: A cartoon illustrating spacer sidewall thickness in single pitch (d) and double pitch (d') regions.	51
Figure 21: Multi-patterning schemes.....	58
Figure 22: CVD/ALD Market Forecast.....	74

List of Tables

	page #
Table 1: Emerging Memory Device Research and Associated Challenges – ITRS	24
Table 2: Emerging Development on Logic Devices – ITRS (source: International Technology Roadmap for Semiconductor, www.itrs.net).....	25
Table 3: ITRS Interconnect Difficult Challenges.....	34
Table 4: 2013 ITRS INTC2- MPU Interconnect Technology Requirements.....	38
Table 5: Precursors By Application	55
Table 6: Applied Materials product line up supporting insulating dielectrics deposition and curing	61
Table 7: TEL product line up supporting insulating dielectrics deposition and curing	62
Table 8: ASM International product line up supporting insulating dielectrics deposition and curing	62
Table 9: Materials & Process Options for 2014, 2016, & 2018.....	67
Table 10: Insulator Precursors: Synthesizers and Suppliers to the IC Market.....	69
Table 11: SOD Precursors/Suppliers	71
Table 12: Korean advanced semiconductor materials suppliers	72
Table 13: The major market participants in the precursor space	77