Status and Future Direction & Strategic Initiative of Taiwan's Semiconductor Industry on AI

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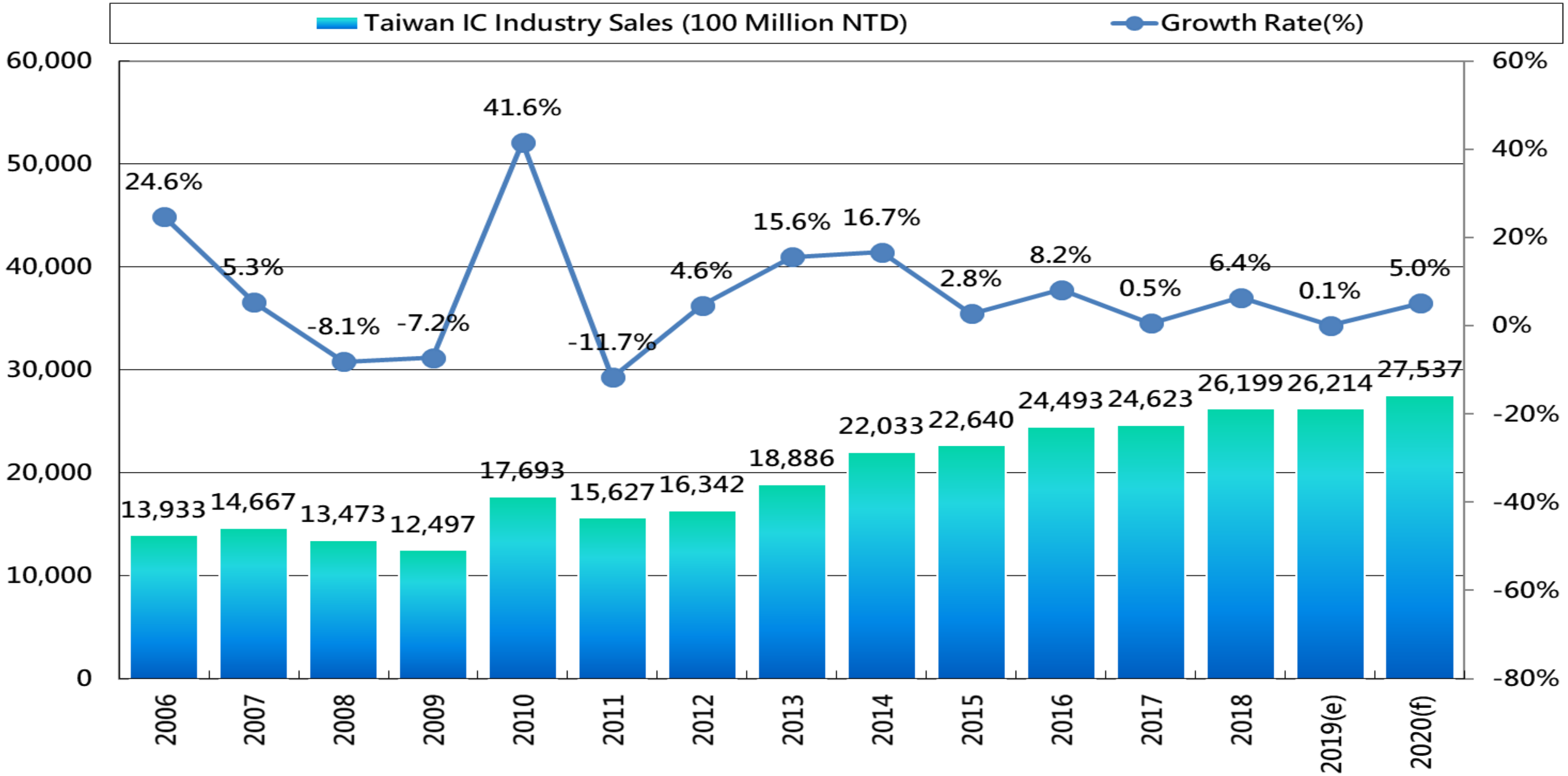
Taiwan's IC Industry Sales is Expected to Reach NT$2,621B (US$87B) in 2019



Taiwan's IC industry in 2019 is expected to reach NT$2,621.4B (US$86.8B) (0.1% growth from 2018), with NT$671.1B by Fabless (US$22.2B) (YoY 4.6% increase), and with NT$1,454.7B by manufacturing (US$48.2B) (Pure Foundry NT$1,306B (US$43.2B) YoY up 1.6%; IDM NT$148.7B (US$4.9B) YoY down 25.8%), and with NT$344.3B by Packaging (US$11.4B) YoY 0.1% decrease, and with NT$151.3B by Testing (US$5B) YoY up 1.9%. Exchange rate NT$/US$ = 30.2

Source: TSIA ; ITRI/ISTI Research

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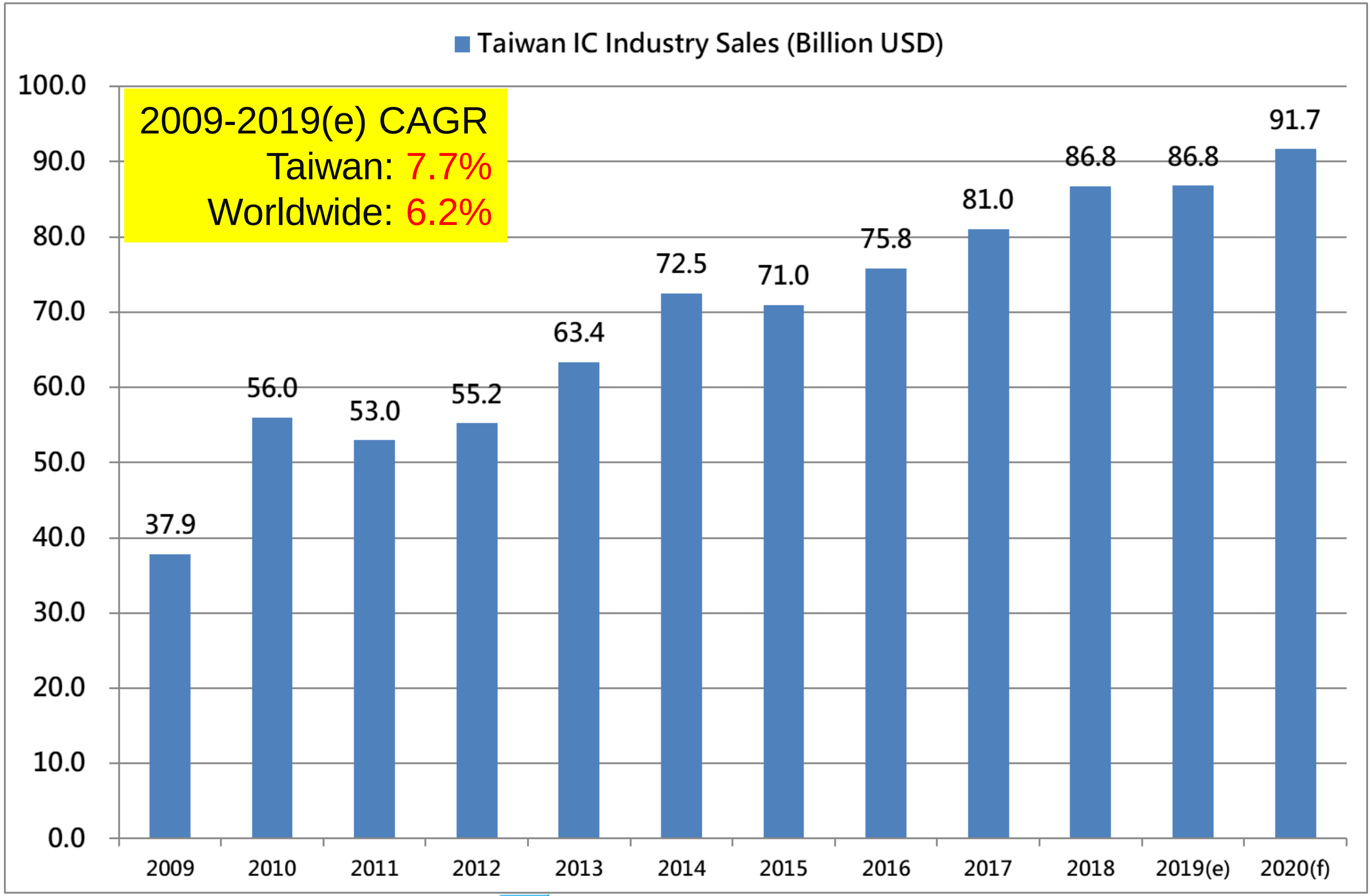
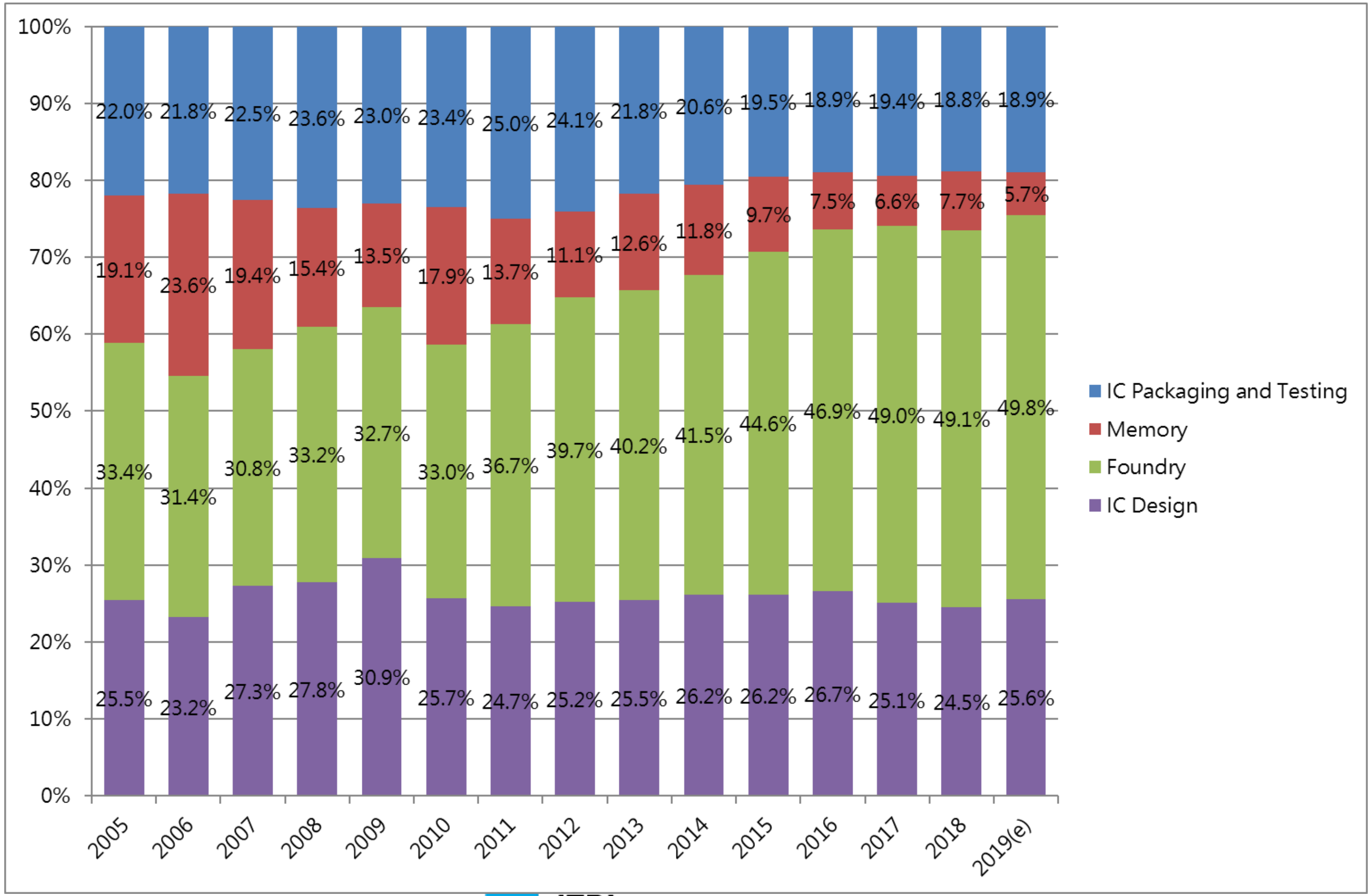
Taiwan's IC Industry Outperform WW with 5.6% Forecasted YoY Growth in 2020



Source: TSIA ; ITRI/ISTI Research

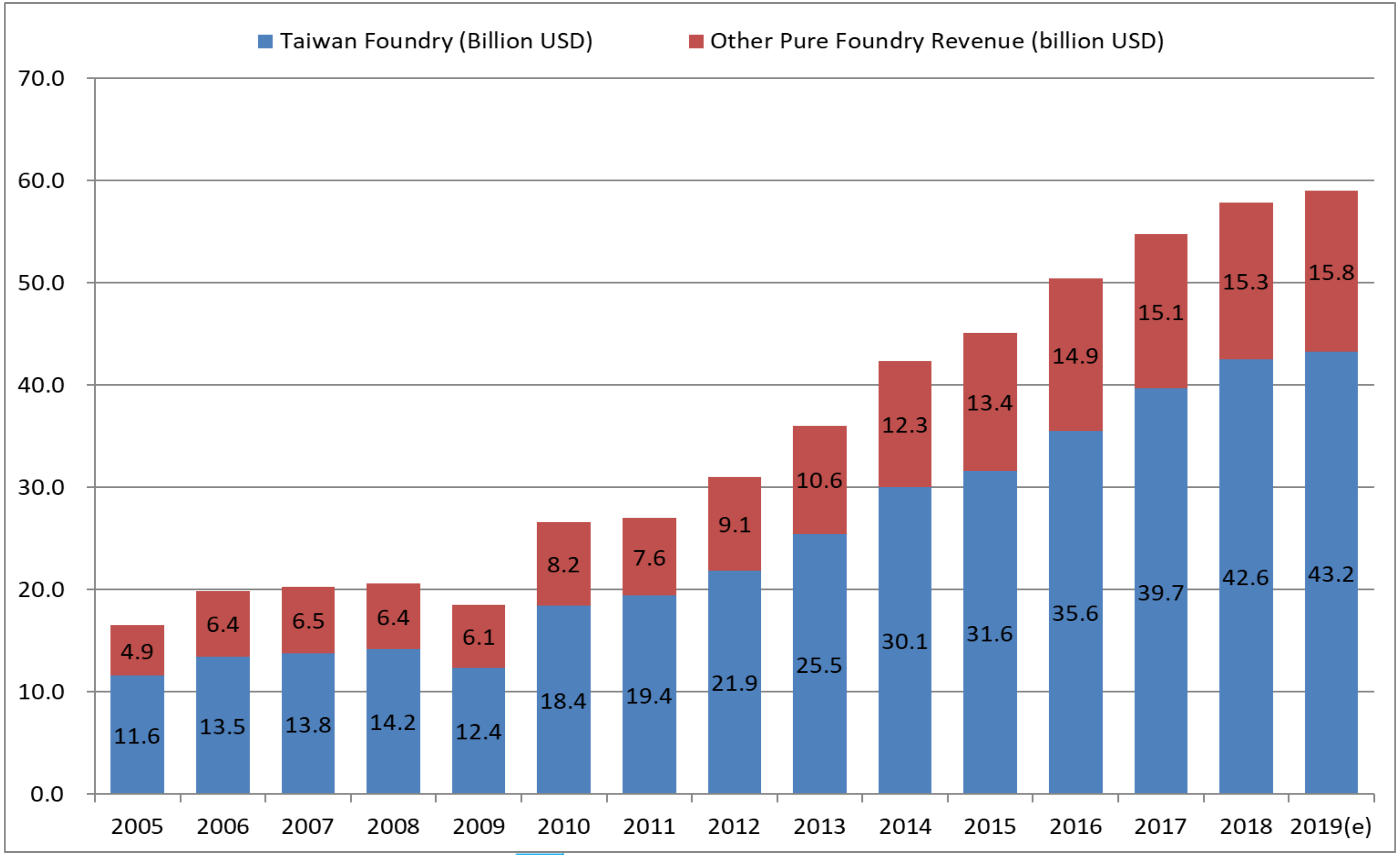
Foundry Business Contributes the Most to Taiwan's Semiconductor Industry, Followed by Fabless

Taiwan semi production value distribution



2019 Taiwan Accounts for 73% of WW Pure Foundry Market

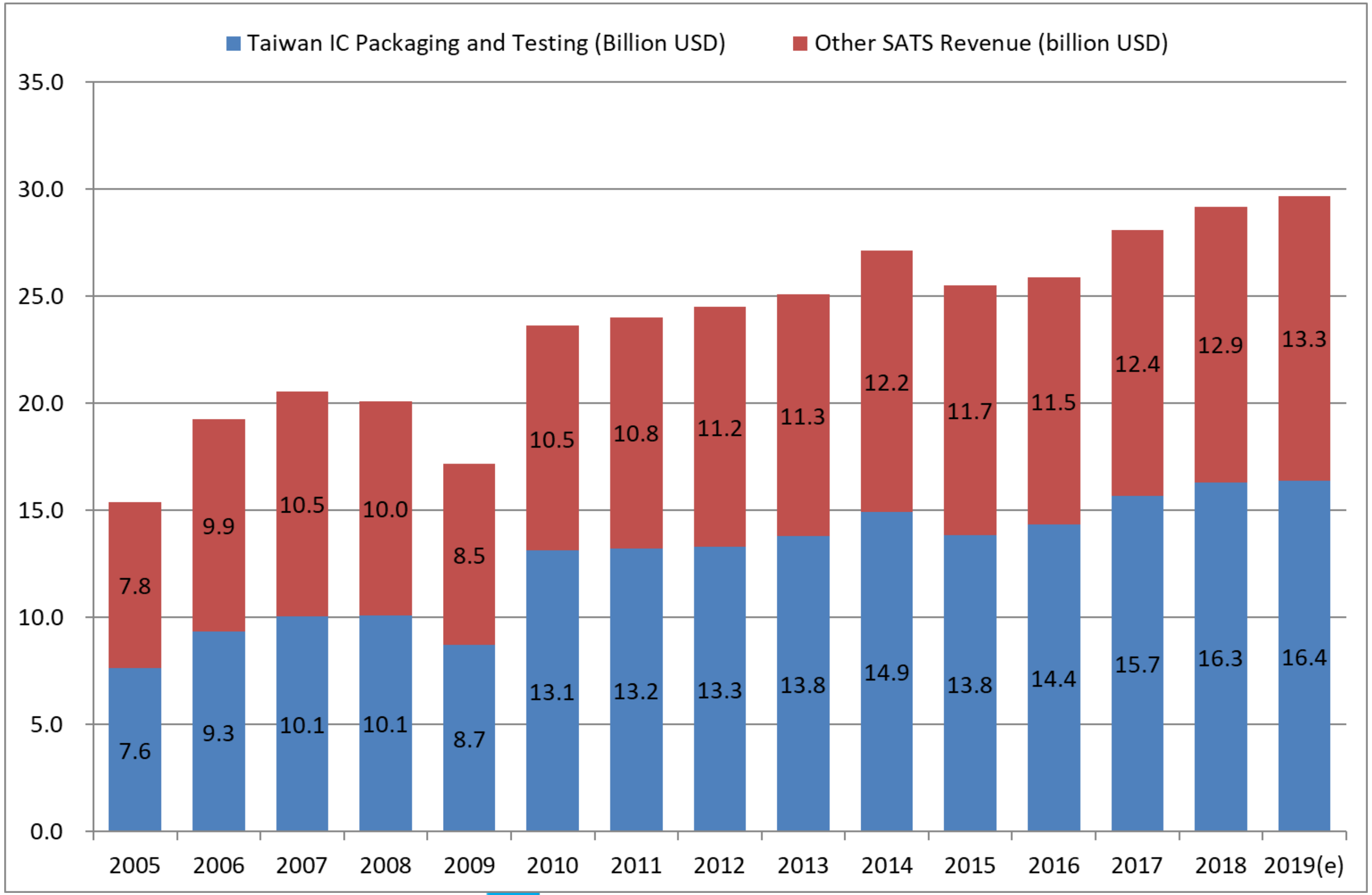
Worldwide Pure Foundry Revenue



Source: TSIA ; ITRI/ISTI Research

2019 Taiwan's IC Packaging & Testing Contributes 55% of Worldwide SATS Market

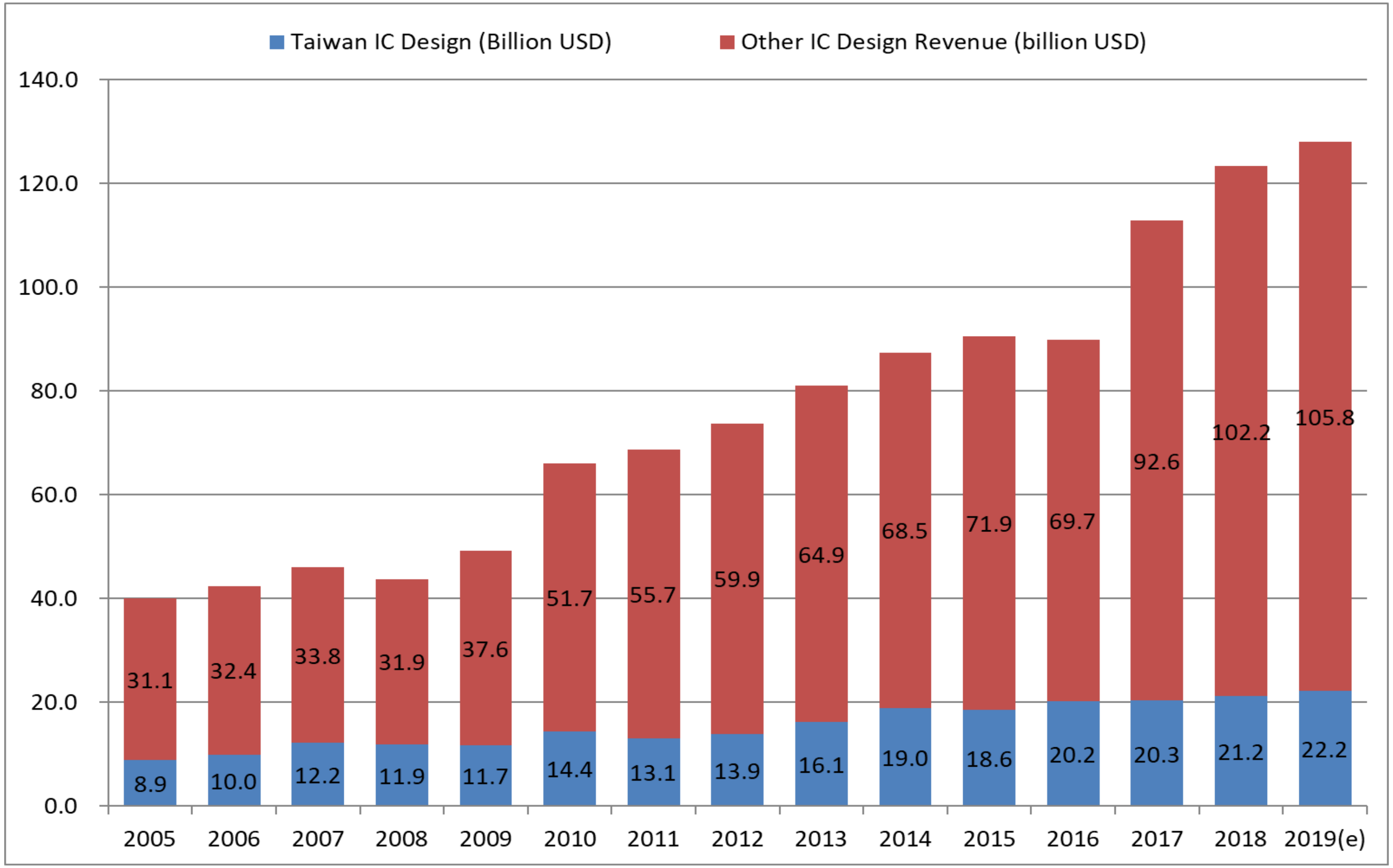
Worldwide SATS Revenue



Source: TSIA ; ITRI/ISTI Research

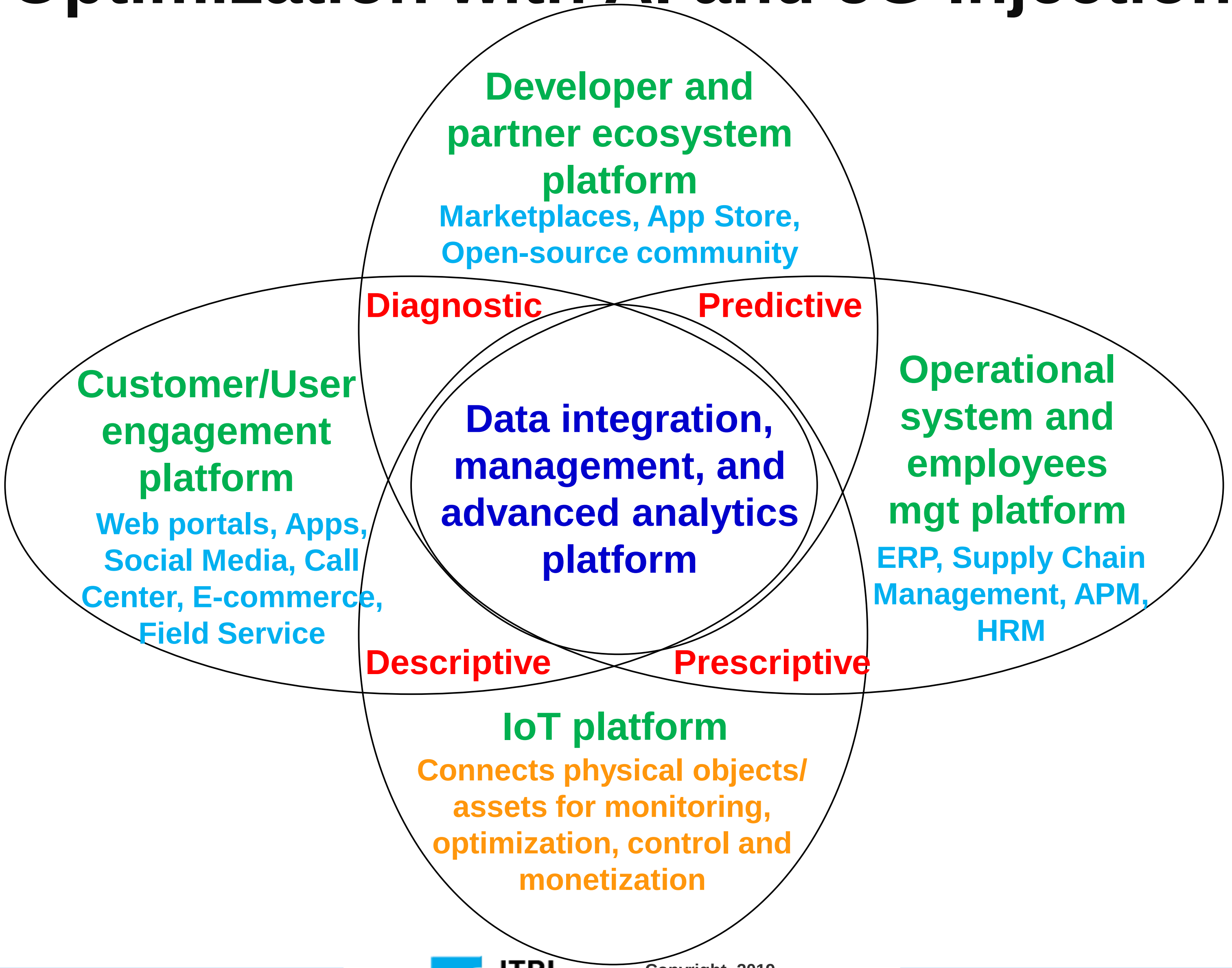
Taiwan's IC Design Industry Needs Strategic Approach to Move up (17% of Worldwide 2019)

Worldwide IC Design Revenue



Source: TSIA ; ITRI/ISTI Research

Five Key Platforms of Digital Business
- Optimization with AI and 5G Injection -

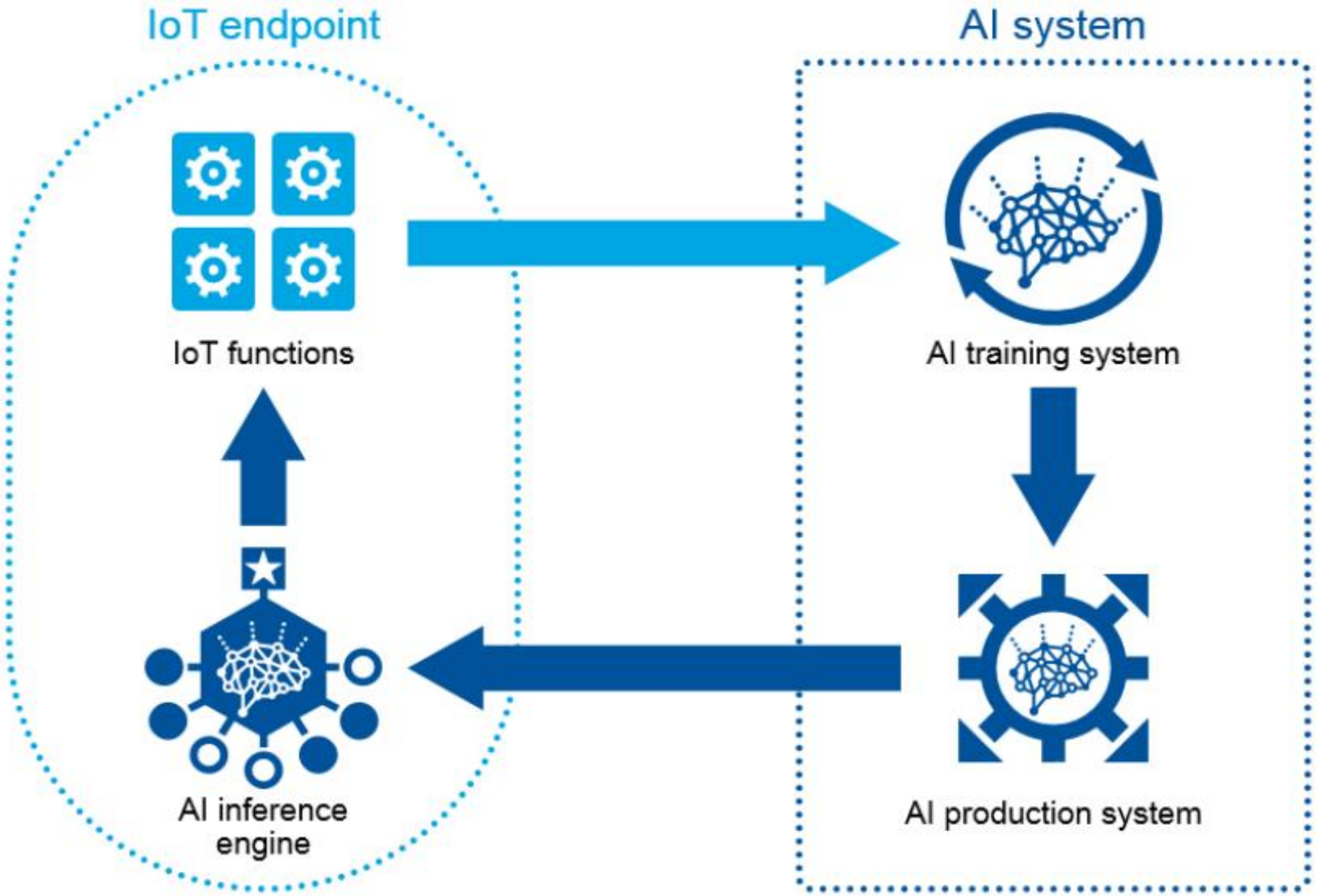


Source: Gartner

5G Free up Bi-directional AI+IoT/Edge System

IoT and AI co-create a virtuous cycle for digital transformation

- IoT's missing puzzle is killer application; on the contrary, AI's missing puzzle is data, making both of which complement with each other.



Source: Gartner

riselab UC Berkeley

NSF An NSF Expedition Project

REAL-TIME INTELLIGENT SECURE EXPLAINABLE SYSTEMS

Current Founding Sponsors

Alibaba Group 阿里巴巴集团 | amazon web services | 蚂蚁金服 ANT FINANCIAL | Capital One | ERICSSON | facebook

FUTUREWEI

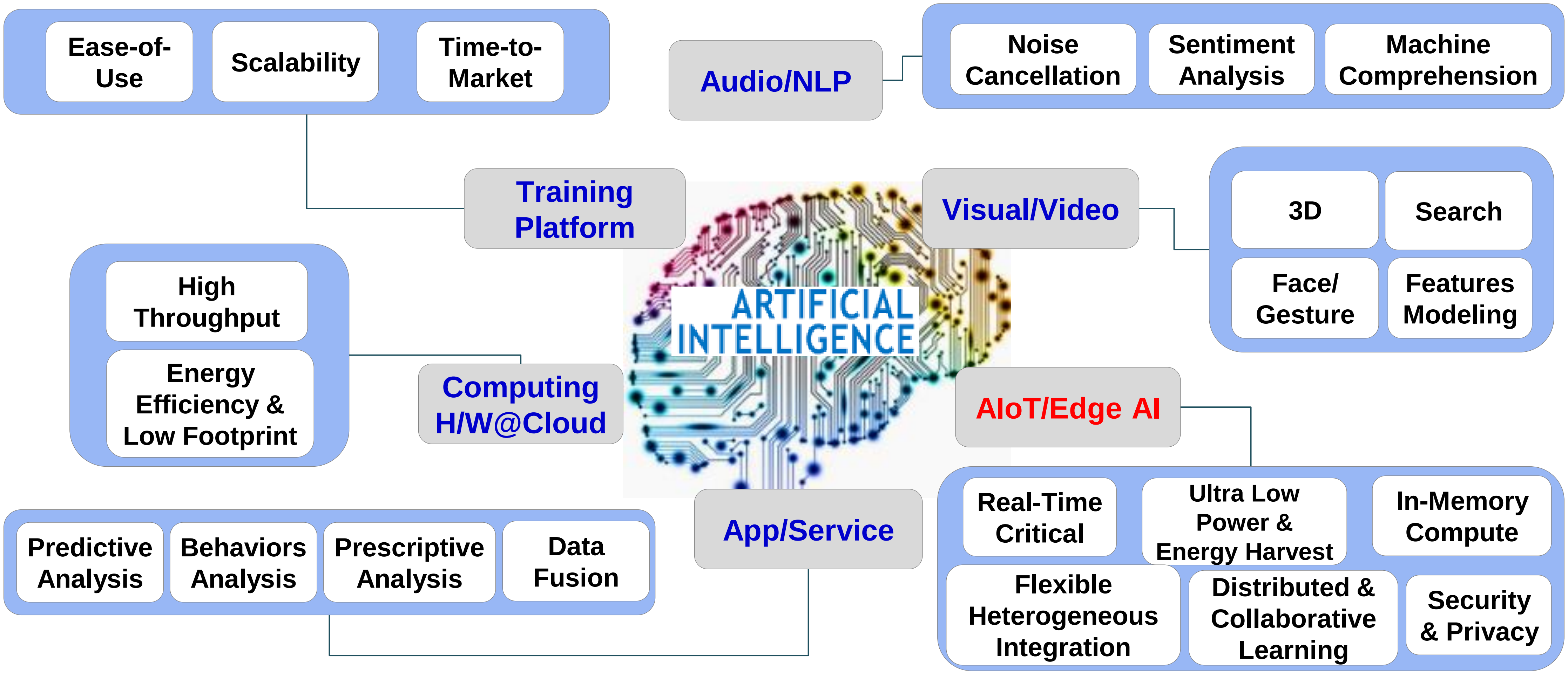
Collaboration between 2 ecosystems of AI and 5G is a must to co-optimize cloud-to-edge systems' performance, cost, and energy efficiency

Google | intel Leap ahead | Microsoft | NVIDIA | Scotiabank | splunk> | vmware

Source: Berkeley RISELab

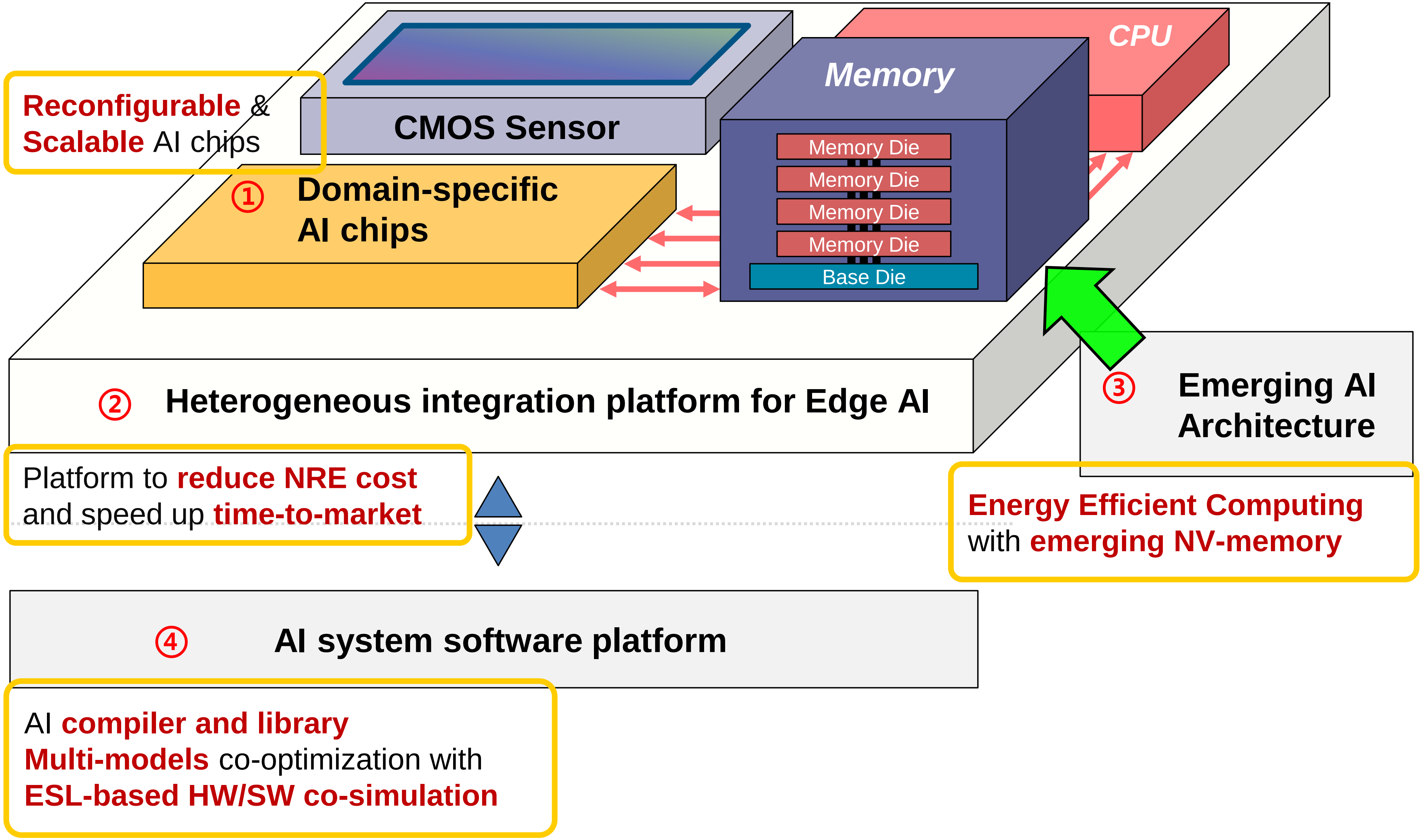
AI Trends and Opportunities
Leveraging 5G to Build a Cloud-Edge Hybrid Model

Collaborative development and co-optimization between hardware and software

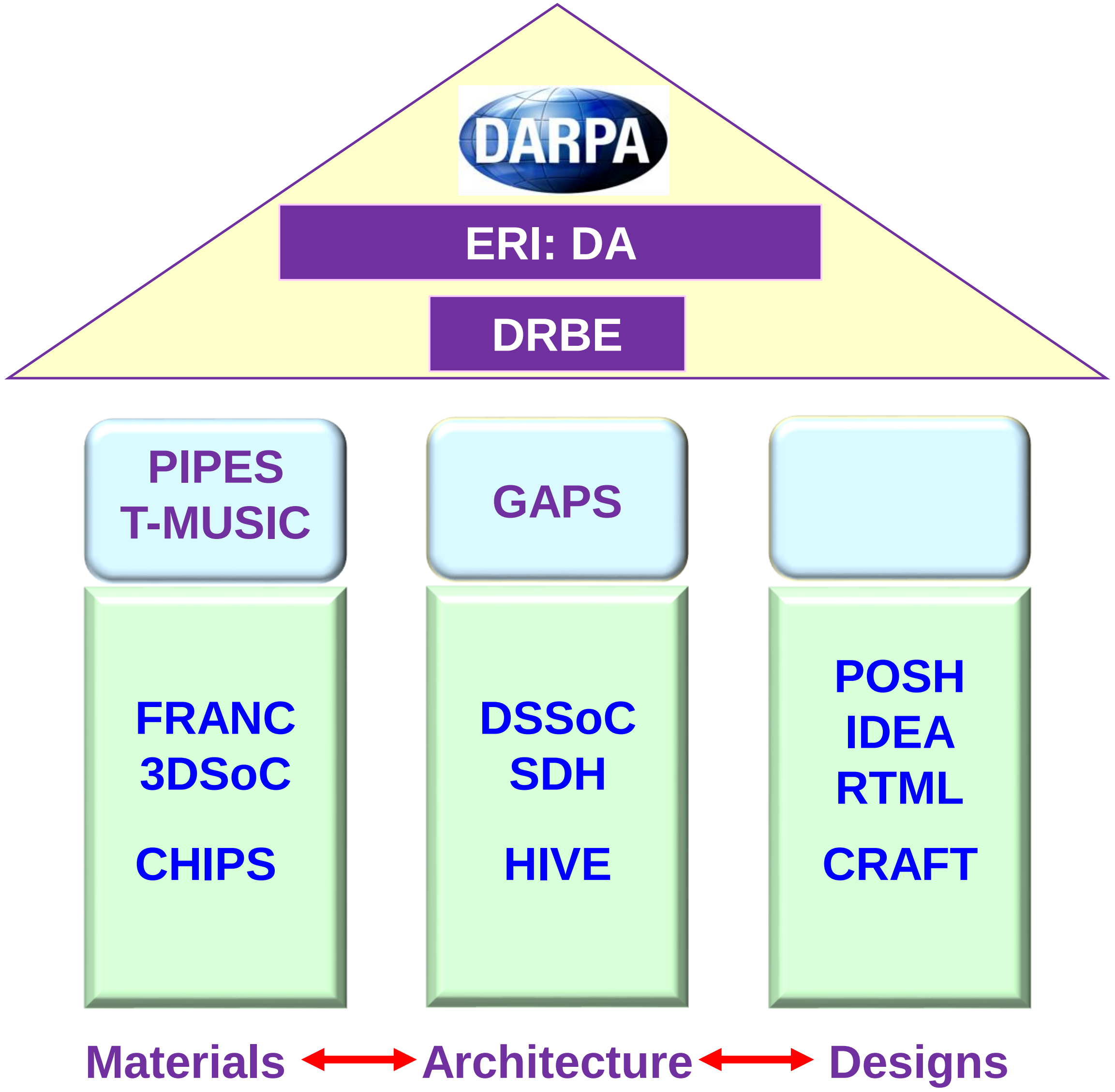


Source: ITRI/ISTI Research

A Funded Initiative and 4-years' AI-on-Chip Program



Benchmark and Look for Partnership with Stakeholders of DARPA Electronics Resurgence Initiative



- DRBE：Digital RF Battlespace Emulator
- PIPES：Photonics in the Package for Extreme Scalability
- T-MUSIC：Technologies For Mixed-Mode Ultra Scaled Integrated Circuits
- GAPS：Guaranteed Architectures for Physical Security
- FRANC：Foundations Required for Novel Compute
- 3DSoC：Three Dimensional Monolithic System-on-a-Chip
- DSSoC：Domain-Specific System on Chip
- SDH：Software Defined Hardware
- POSH：Posh Open Source Hardware
- IDEA：Intelligent Design of Electronic Assets
- RTML：Real Time Machine Learning
- CHIPS：Common Heterogeneous Integration and IP Reuse Strategies
- HIVE：Hierarchical Identify Verify Exploit
- CRAFT：Circuit Realization At Faster Timescales

Source: DARPA

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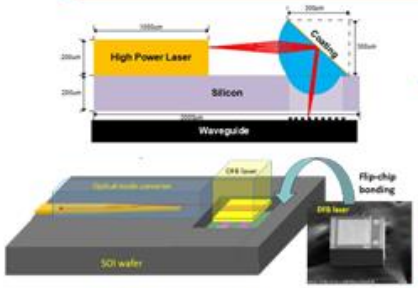
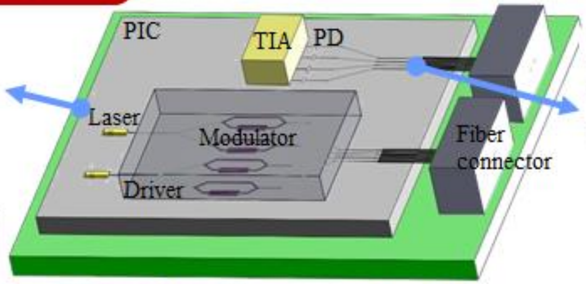
ITRI Addressing the Need for Low-cost and Volume-scalability Si-Photonics PKG & Test Opportunities

Focus on optical I/O packaging, laser diode integration, silicon photonics IC integration and testing

PIC packaging platform (Laser)

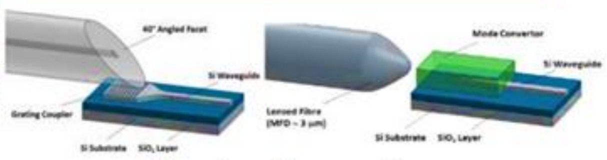


Laser integration

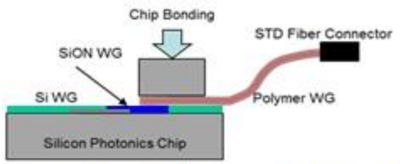


Multi-channel silicon photonics transceiving module

PIC packaging platform (Fiber & Polymer WG)

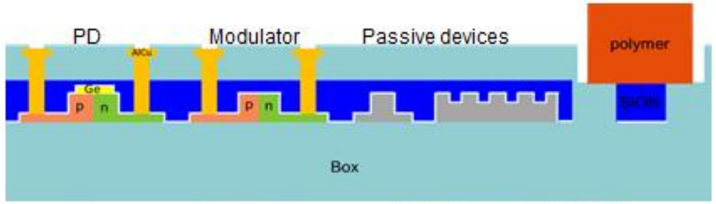


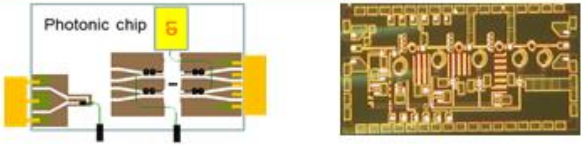
Low loss fiber coupling



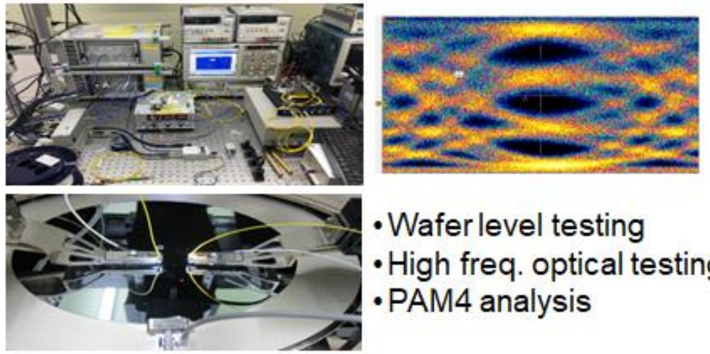
Multi-channel polymer WG array (Fan-out)

EIC+PIC integration





High speed testing platform



- Wafer level testing
- High freq. optical testing
- PAM4 analysis

Source: ITRI

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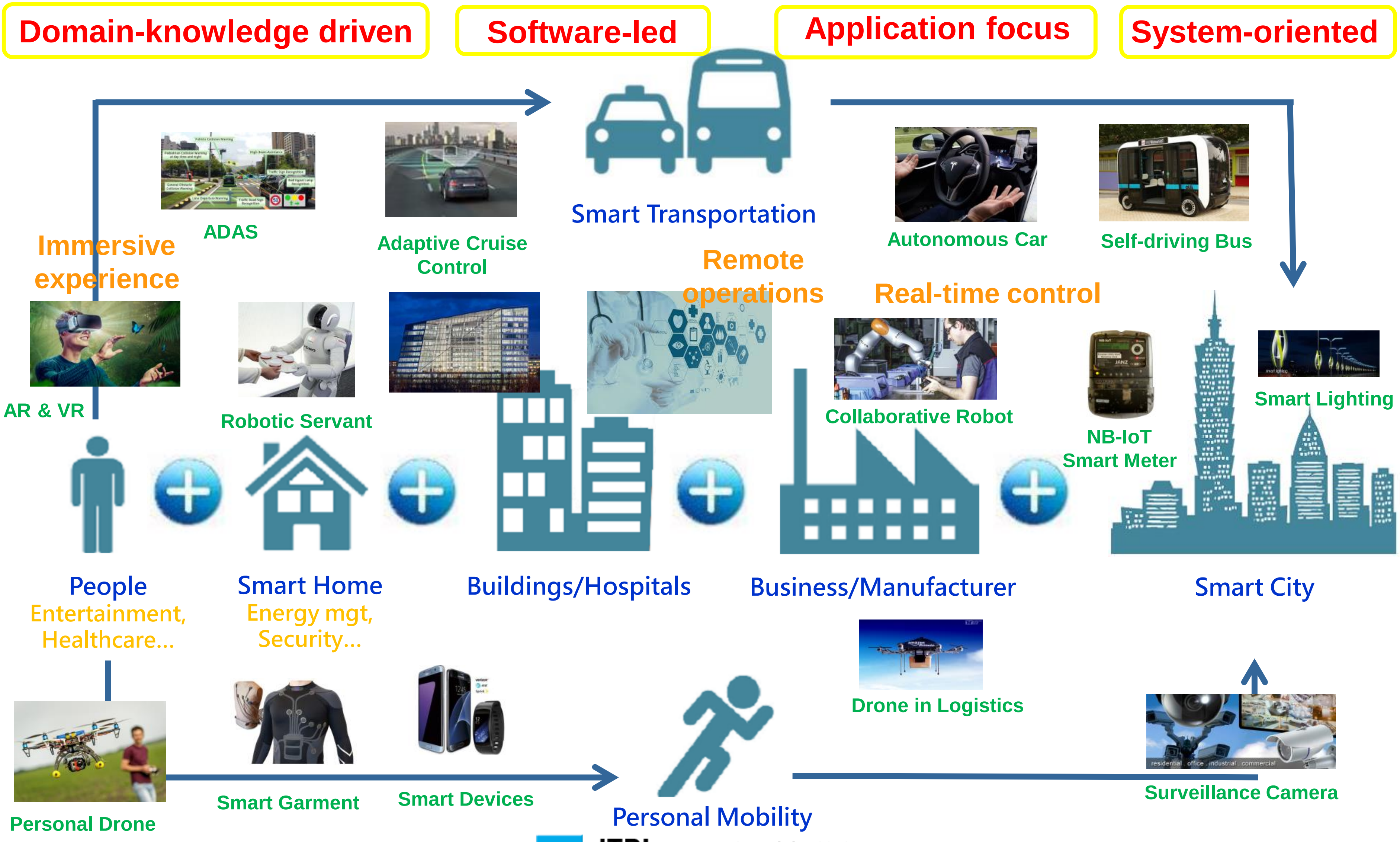
Use-case-driven AIoT in Verticals under 5G Context Pose Challenges to Semi Industry

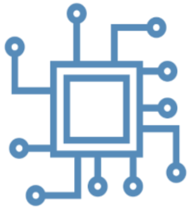


Source: ITRI/ISTI Research

AI on Chip Taiwan Alliance (AITA)

Creating AI Business Opportunities

- ■Integrating AI Chip and applications into an AI eco-system
- ■Connecting the enterprise with startups
- ■Attracting more investments from industries



Created by Aiden Icons
from Noun Project

Developing Key Technologies

- ■Industry establishes SIG
- ■Leverage academy, research-institute and industrial research capability

Created by Alina Oleynik
from Noun Project

Accelerating Product Development

- ■Develop the specs. for common interface
- ■Create a platform for long term investments

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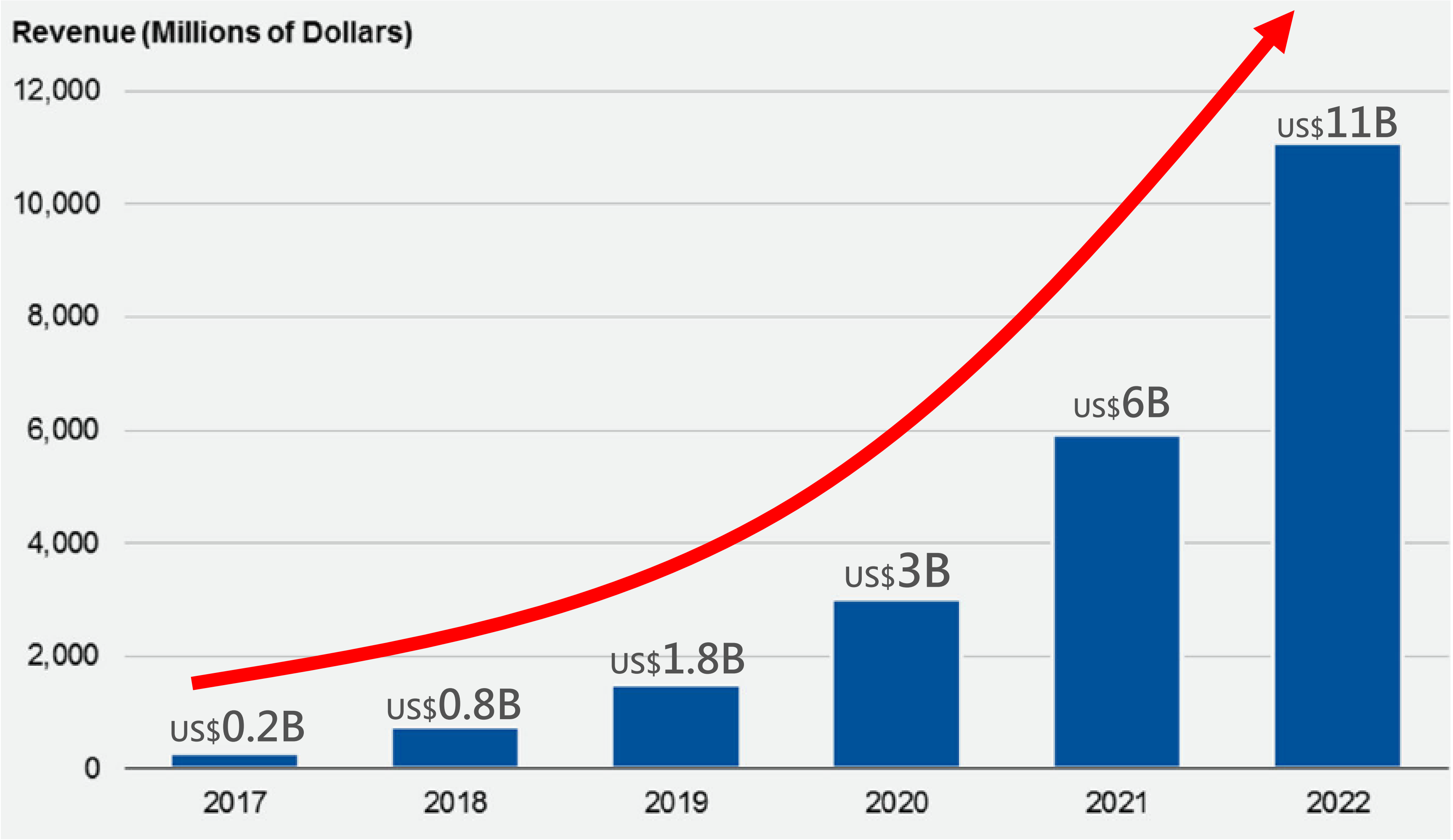
Global Edge AI Chip Market Expected to Grow Exponentially and Exceed US$30B in 2025

By 2023, over 20% of revenue from ASSPs and ASICs within IoT endpoint or edge device will have local AI functionality and capability



Source: ITRI/ISTI Research

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Benefits to Semiconductor Industry by AI Deployment

1 Predictive Maintenance
- Data from multiple sources is sent to AI engine
- Machine learning (ML) algorithms predict equipment maintenance needs
- Workers execute suggestions for maintenance

2 Yield Improvement
- Data from fabrication equipment, e-test, in-line defects, etc., is sent to AI engine
- ML algorithms analyze data to predict source of yield issues
- Engineers execute decisions for yield improvement based on this analysis

3 Operational Efficiency
- Test data across entire manufacturing process is fed into AI engine
- ML algorithms analyze this data to predict chip performance
- Engineers use this analysis to reduce costly final tests and make product ship decisions

4 IC Design Optimization
- Integrated circuit (IC) design is fed to AI engine
- ML algorithms predict design issues that could lead to systematic defects
- Designers make appropriate design changes to eliminate potential issues

5 Automated Inspection
- Microscopes in the fab combine nanoscale imaging with AI
- ML algorithms detect new defects and pass information across tools in the fab
- Engineers can focus on identified defects without spending time on manual inspections

Source: Gartner

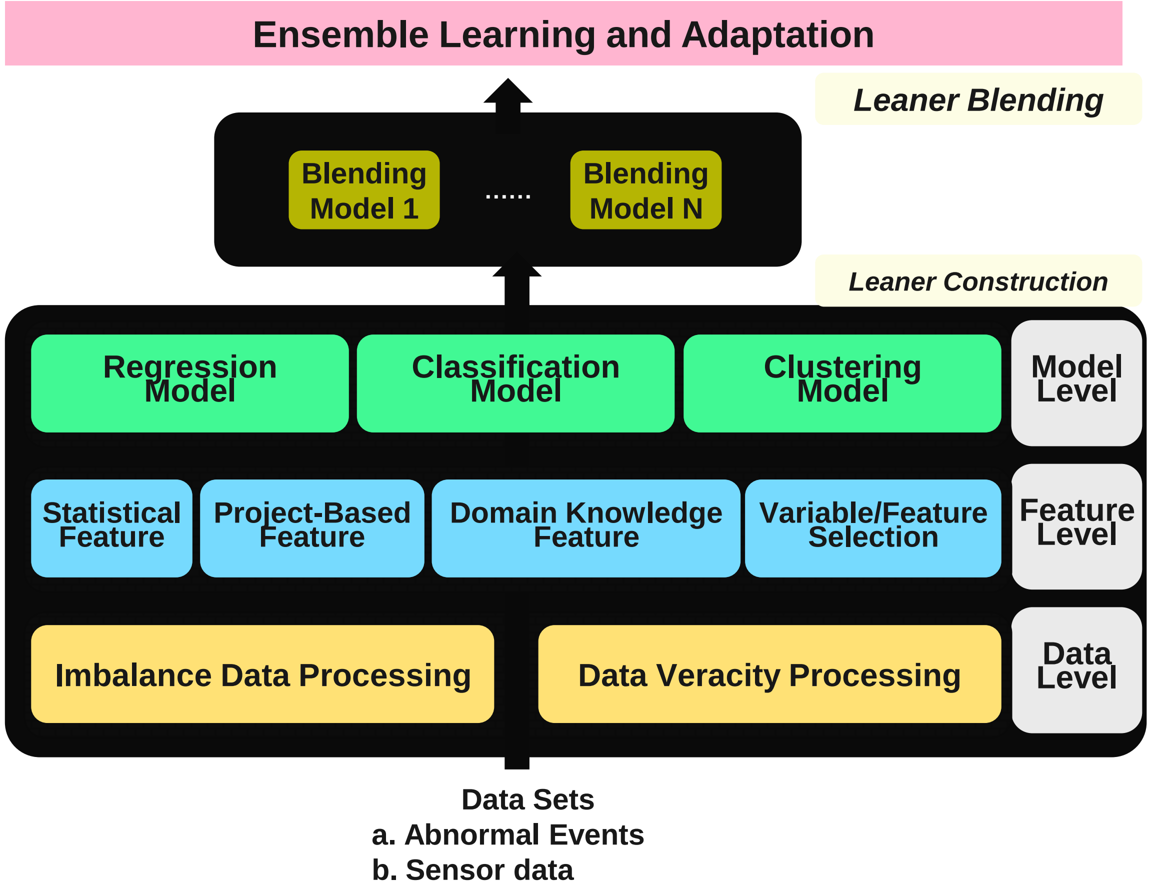
Prognostic and Health Management by ITRI for Semi Industry

- *PHM is based on AI and machine learning which analyzes the processing data generated by machines & monitors and predicts in real time as well as presents with visualized insights.*

Requirements : Fault/Failure prognosis for semiconductor manufacturing

Data Visualization

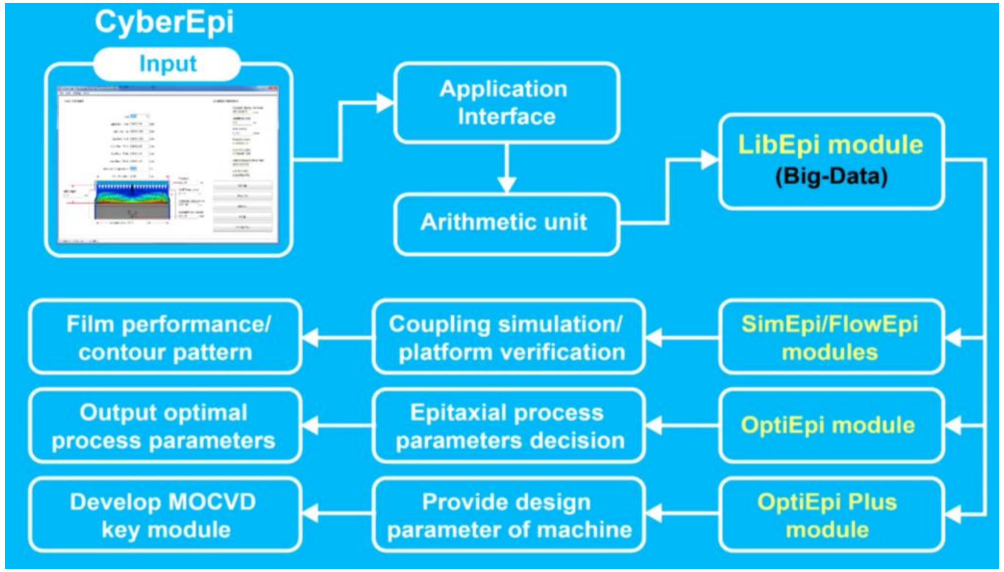
Four levels of PHM's primary technology operating flow



ITRI Case : CyberEpi Optimizes Epitaxial Process

- CyberEpi is a software through multi-physical and chemical coupling simulation analysis, as well as heat flow field visualization technology
- CyberEpi can reduce control time of the epitaxial process, from weeks to hours which formerly required and performed only by epitaxy expert with try-and-error endeavor
- CyberEpi serves as a Digital Twin of MOCVD system; shortens R&D and product launch cycle of LEDs, solar cells, and high-power integrated circuits

CyberEpi Operation Architecture



CyberEpi Performance Index

	Traditional → CyberEpi	Improve
Control time	Reduction 1 Week → 2 hours	98% ↑
Uniformity (Epitaxial Process)	Increase 92% → 95%	3% ↑
Time to market	Faster 3 Month → 1 Month	66% ↑

Source: ITRI

Manufacturing Big Data Analytics to derive control rules for cycle reduction

IEEE TRANSACTIONS ON AUTOMATION SCIENCE AND ENGINEERING 1

Manufacturing Intelligence to Exploit the Value of Production and Tool Data to Reduce Cycle Time

Chung-Jen Kuo, Chen-Fu Chien, *Member, IEEE*, and Chen-Tao Chen

***Abstract*—Cycle time reduction is crucial for semiconductor wafer fabrication companies to maintain competitive advantages as the semiconductor industry is becoming more dynamic and changing faster. According to Little's Law, while maintaining the same throughput level, the reduction in Work-in-Process (WIP) will result in cycle time reduction. On one hand, the existing queueing models for predicting the WIP of tool sets in wafer fabrication facilities (fab) have limitations in real settings. On the other hand, little research has been done to predict the WIP of tool sets with tool dedication and waiting time constraint so as to control the corresponding WIP levels of various tool sets to reduce cycle time without affecting throughput. This study aims to fill the gap by proposing a manufacturing intelligence (MI) approach based on neural networks (NNs) to exploit the value of the wealthy production data and tool data for predicting the WIP levels of the tool sets for cycle time reduction. To validate this approach, empirical data were collected and analyzed in a leading semiconductor company. The comparison results have shown practical viability of this approach. Furthermore, the proposed approach can identify and improve the critical input factors for reducing the WIP to reduce cycle time in a fab.**

changing faster in consumer era. Therefore, time-to-market and cycle time reduction have become increasingly critical issues for both research and practice.

According to Little's Law, while maintaining the throughput level of individual tool sets in a fab, reducing the WIP levels will reduce the cycle time. There is a gap to effectively determine appropriate Work-in-Process (WIP) levels for various tool sets in a fab in light of dynamic nature of wafer fabrication and complicated product mix on line. Indeed, a number of queueing and simulation models have been developed in predicting the WIP or the cycle time of tool sets in a fab. However, most of the studies applying queueing models have limitations in real settings due to the requisite assumptions to which few real-world systems conform [1], [2]. In particular, conventional queueing theory assumes all the servers are identical in a service center. However, tool dedication constraint for wafer fabrication requires that certain tools in a tool set can process only part of products or processing steps. That is, the tools in the tool set are not identical

Factor	Relation with WIP	% of tool sets conform to the relation	Sensi-tivity ratio	Managerial implications
m	−	92%	0.83	--
u	−	93%	0.28	To relax tool dedication for non-critical products
λ	+	95%	1.06	--
C_a	+	87%	0.38	To smooth hour-to-hour lot arrivals
v	−	94%	1.37	To improve tool availability
D_v	+	73%	0.28	To balance non-available tool events among hours
s_0	+	86%	0.77	To shorten process time
C_{s0}	+	79%	0.18	To evaluate effect of merging similar recipes on WIP
l	+	81%	0.44	To merge or split lots until the mean lot size approach the optimal level
D_l	+	88%	0.24	
b	−→+	83%	0.72	To develop model to determine the optimal batch size by recipes
D_b	+	76%	0.37	
r	+	75%	0.46	To simplify number of recipes
rw	−	82%	0.22	To eliminate unnecessary waiting time constrains
tw	−	88%	0.56	To relax the specification for waiting time constraint

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Taiwan's Semiconductor Ecosystem Attracts Foreign Partners

Microsoft
Micron
ASML
CORNING
LINTEC
arm
SYNOPSYS®
Google
ShinEtsu
QUALCOMM®
Mitsui Chemicals
intel®
APPLIED MATERIALS®
Hitachi Chemical
Heraeus

Source: ITRI/ISTI Research

Thank You

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