Wafer Surface Control Evolving Specifications

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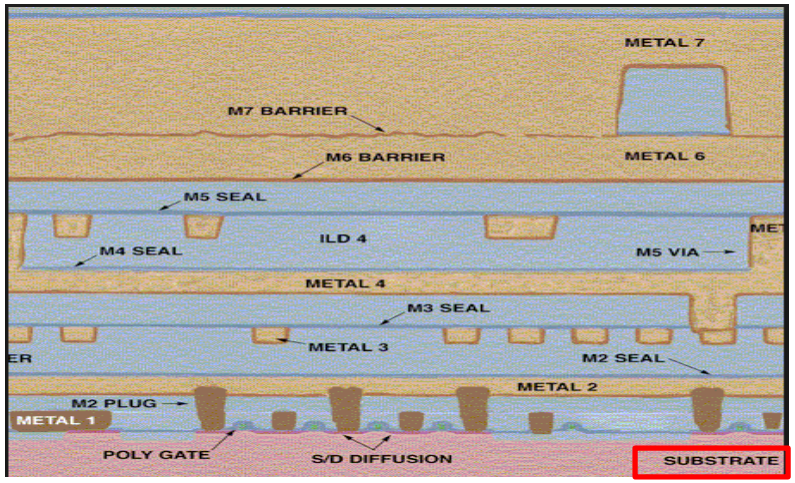
Overview

- Introduction
- What is our FAB Strategy?
- Critical parameters for FAB performance
  - Incoming wafer PC
  - Wafer Flatness
- Future Challenges

Introduction

IC Manufacturing



http://lamp.tu-graz.ac.at/~hadley/nanoscience/week5/5.html

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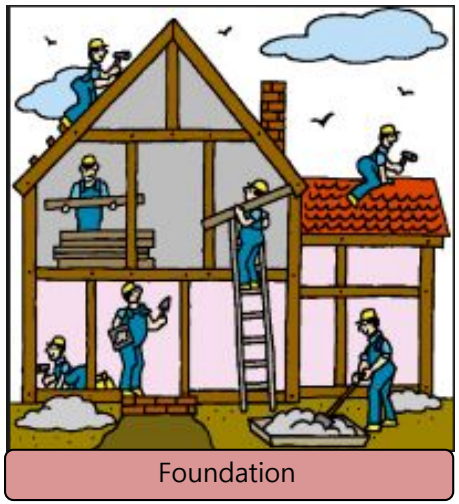
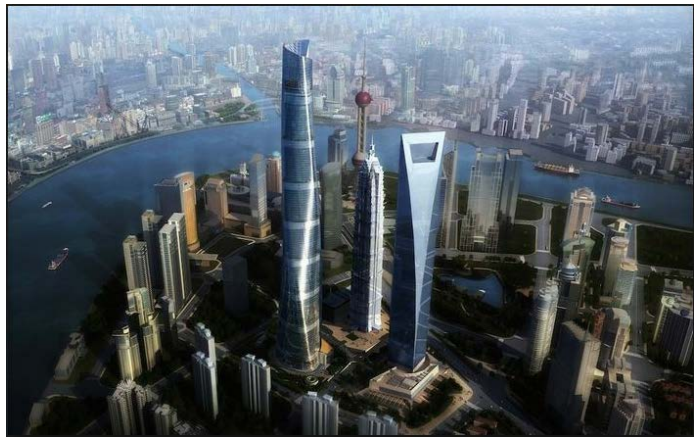
Build House



Sound Foundation is critical !!
Wafer = Foundation

Introduction

https://www.beazer.com/maryland--dc-md/quarry-place---single-family-homes

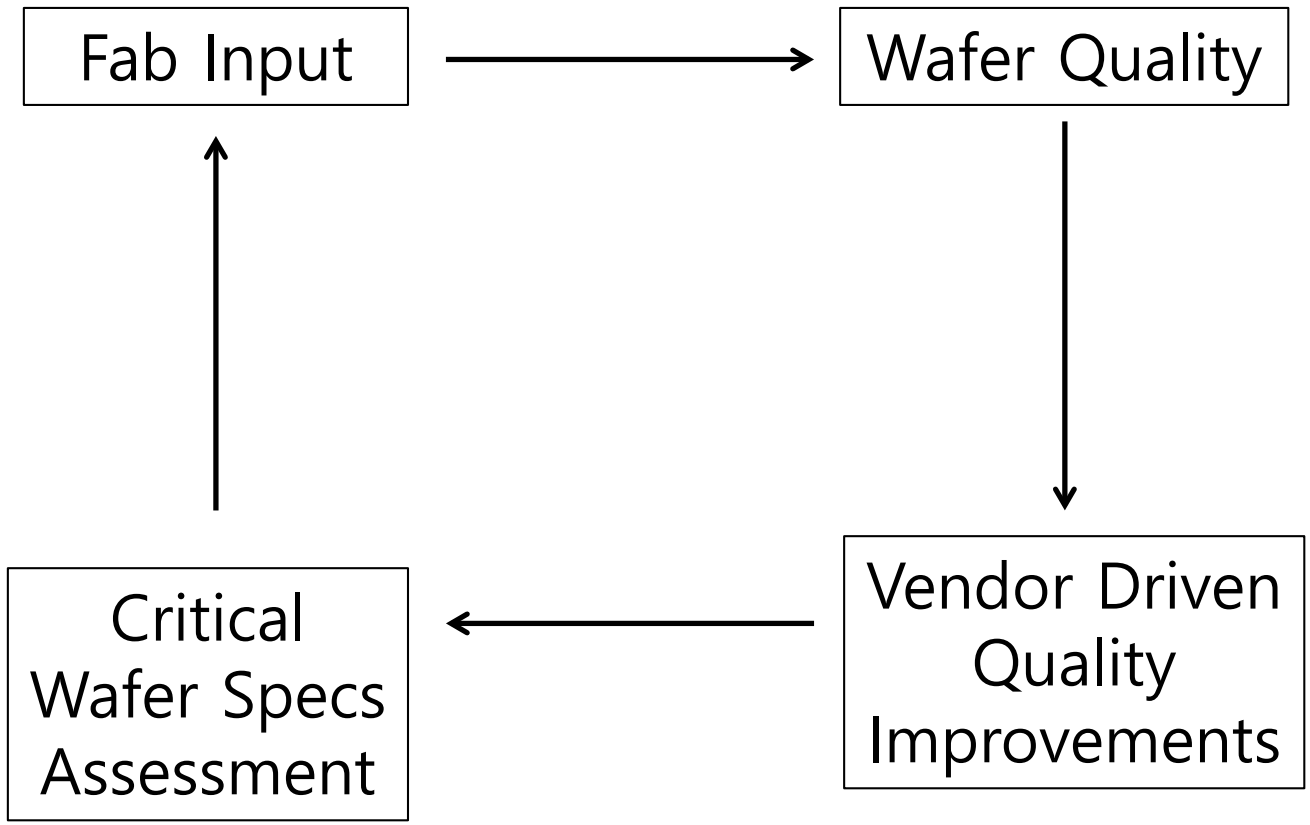


http://photovide.com/10-weird-buildings/

Planar FinFet and beyond

- Newer device structures → tighter wafer specs and control
  - Key wafer parameters and related fab signals
    - There is still lot of room for improvement
  - Future challenges to wafer manufacturers
    - Are we are currently flying blind ?
    - Think Differently

Fab Strategy



Fab Strategy

Focus on two key wafer parameters
(a) Incoming wafer PC (b) Wafer Flatness

- Both included in wafer related ITRS Roadmap
- Both behind what advanced nodes need as per ITRS*

ITRS Roadmap for critical particle size

Year of Production	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*	*2023*	*2024*	*2025*	*2026*	*2027*	*2028*
DRAM ½ Pitch (nm) (contacted)	24	22	20	18	17	15	14	13	12	11	10	9.2	8.4	7.7
Critical particle size (nm) based on 50% of DRAM 1/2 Pitch (nm (contacted) [1]	12	11	10	9	8.5	7.5	7	6.5	6	5.5	5	4.6	4.2	3.9

ITRS Roadmap for wafer site flatness

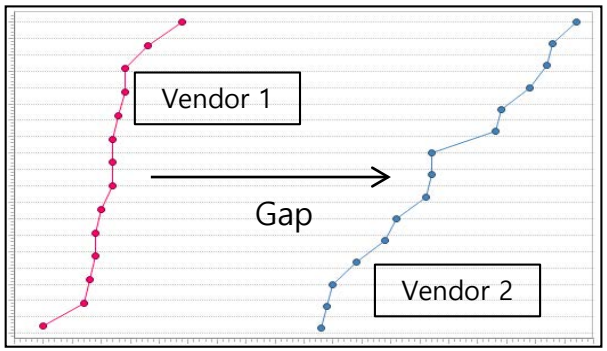
Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
Site flatness (nm), SFQR 26 mm × 8 mm site size	80	70	65	57	45	42	36	35	32

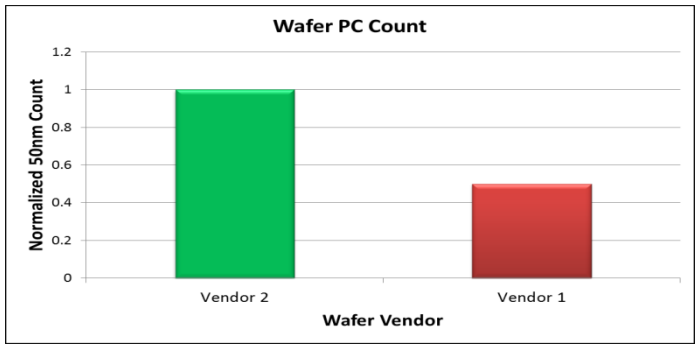
*** ITRS standards are referred here as a guide for bare wafers but in reality specs requirements are even tighter than that.**

Critical Parameters for FAB Performance

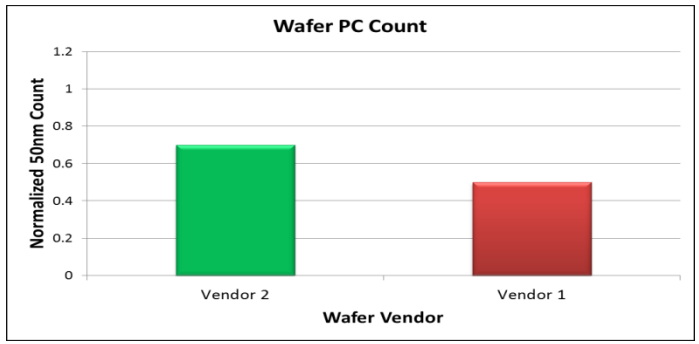
Critical Wafer Quality: PC

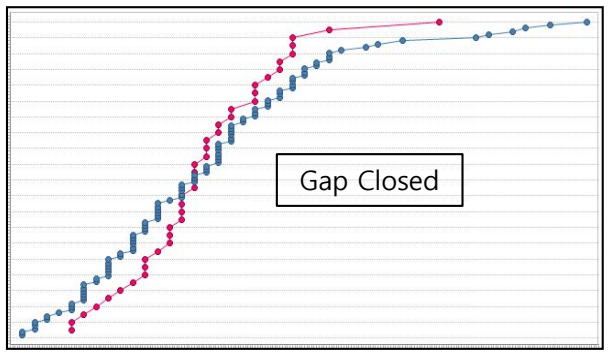
Post pad film defects highlight incoming material quality





Vendor Actions

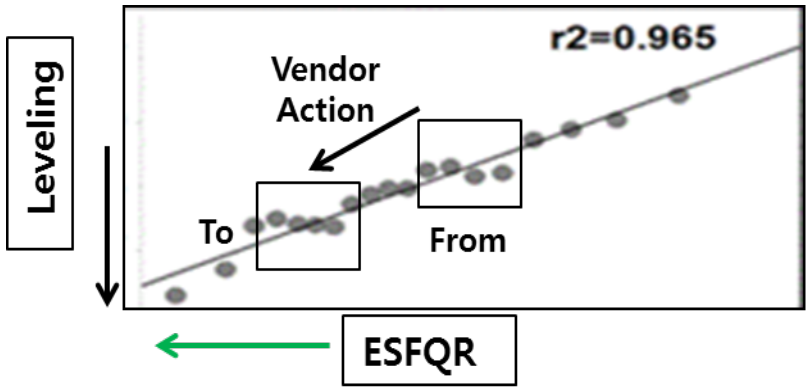




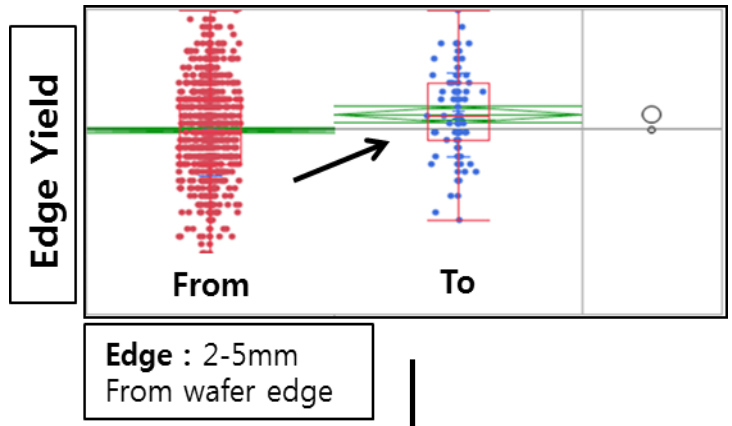
Fab: Support supplier improvements with FAB input
Vendor: Drive actions to close highlighted quality gap

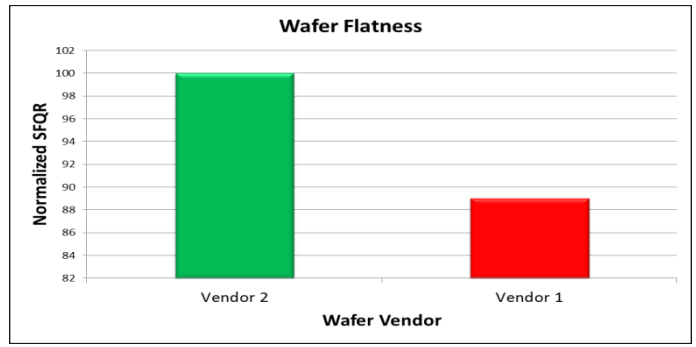
Critical Wafer Quality: Flatness

Photo leveling dependence on wafer edge flatness



ESFQR: Edge Site Flatness Least Squares





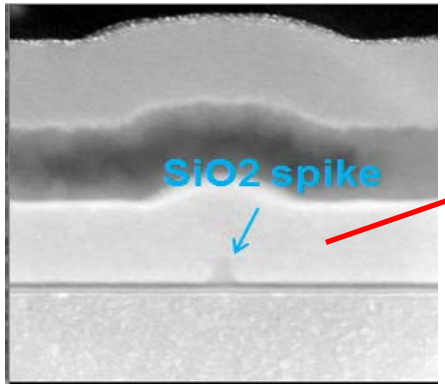
Work in Progress

Fab: Identify and understand critical wafer quality parameters dependence on fab performance, feedback to vendor for quality improvement

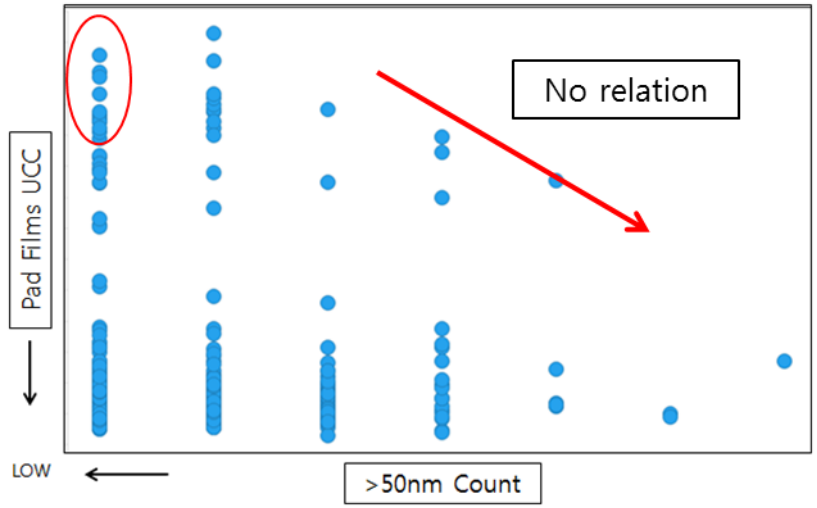
Vendor: Identify process knobs to achieve the desired improvement

Challenges to Wafer Vendor

Challenges to Wafer Vendor



Defect on High flyer wafers post pad films

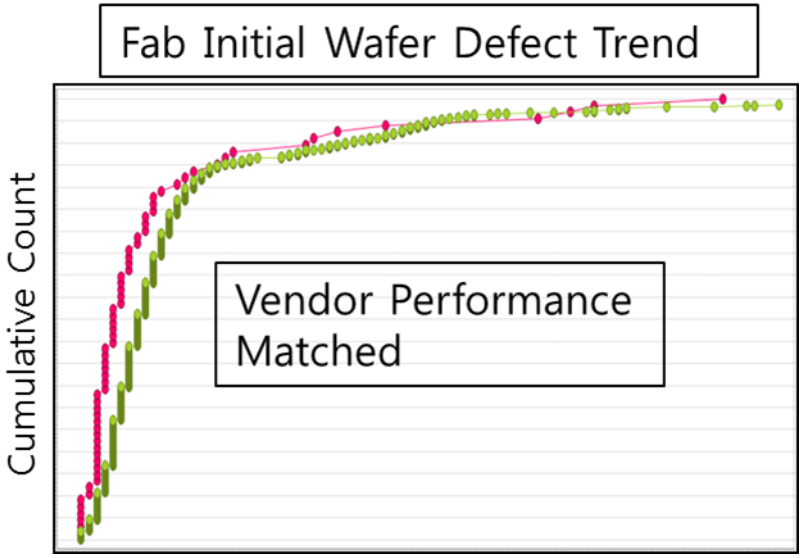


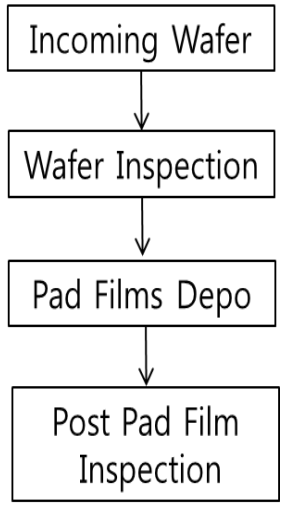
Incoming CoA not catching wafer related defects.

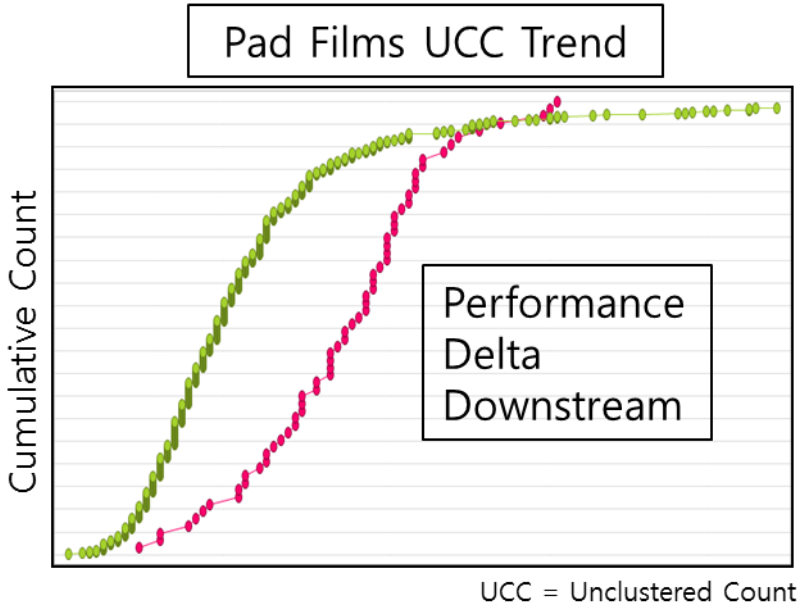
- 50nm PC spec obsolete for advanced nodes.
- Need to monitor and spec lower PC bins
  - Which pc size is appropriate ? 37nm, 26nm, 19nm ?
  - Vendors need to install SP5 capability and capacity.

Challenge: Install appropriate PC monitoring capability and capacity for advanced nodes ?

Challenges to Wafer Vendor



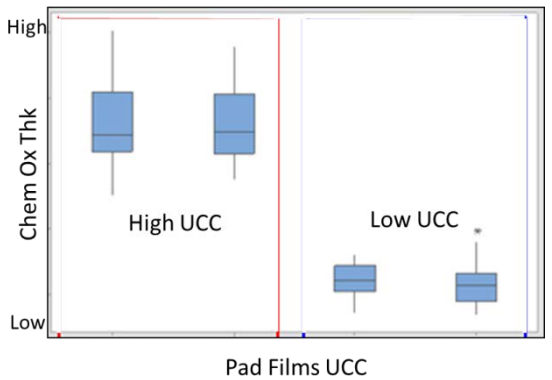




Monitoring traditional wafer quality parameters is not enough.

- Monitor chemical oxide thickness ?

Use non-traditional techniques like deposition of decorating films to monitor and improve wafer quality

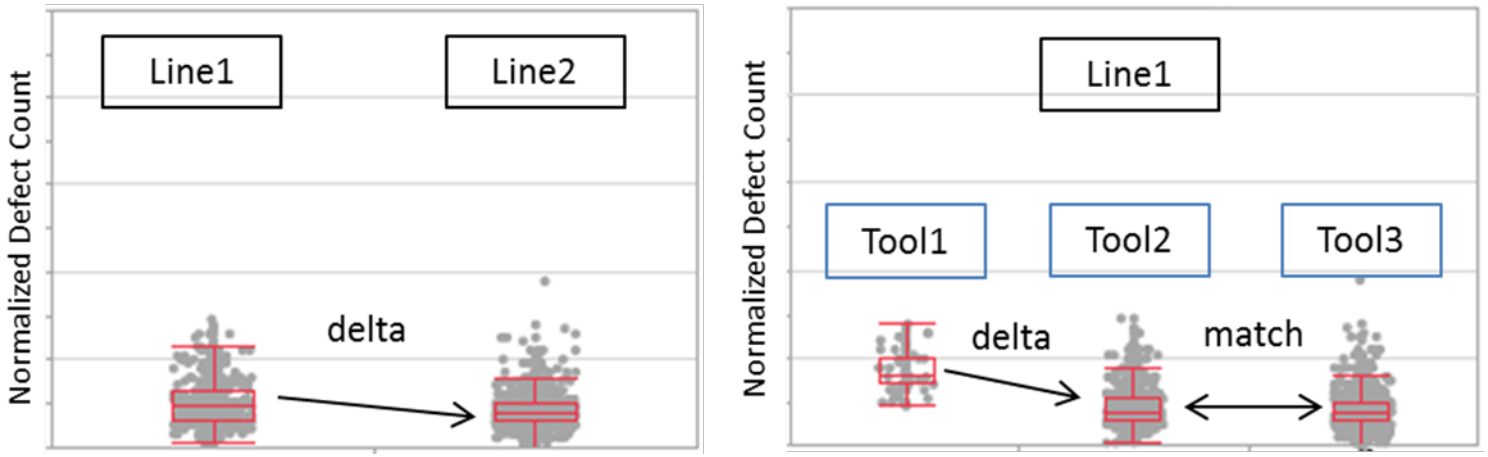


Challenge: Monitor non-traditional wafer parameters,
Use non traditional techniques to improve quality

Challenges to Wafer Vendor

Wafer Vendor raw material/site matching Impact on Quality

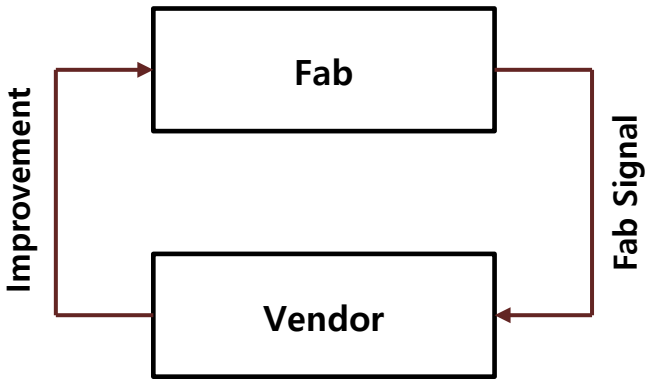
- How well do you monitor incoming chemical quality ?
- How well do you monitor site UPW quality ?
- Do you have the right chemical quality monitoring capability?
- Tool to tool matching or manufacturing line to line matching ?



Challenge: Think like a HVM Fab

Summary

"Appropriate" wafer quality is critical for advanced nodes to be successful



Collaborate

Continuous Improvement

Think Differently

THANK YOU