TECHCET

Electronics Materials Information

MATERIALS ROADMAPS FOR ADVANCED SEMICONDUCTOR DEVICES:
MATERIAL MARKET TRENDS & OPPORTUNITIES

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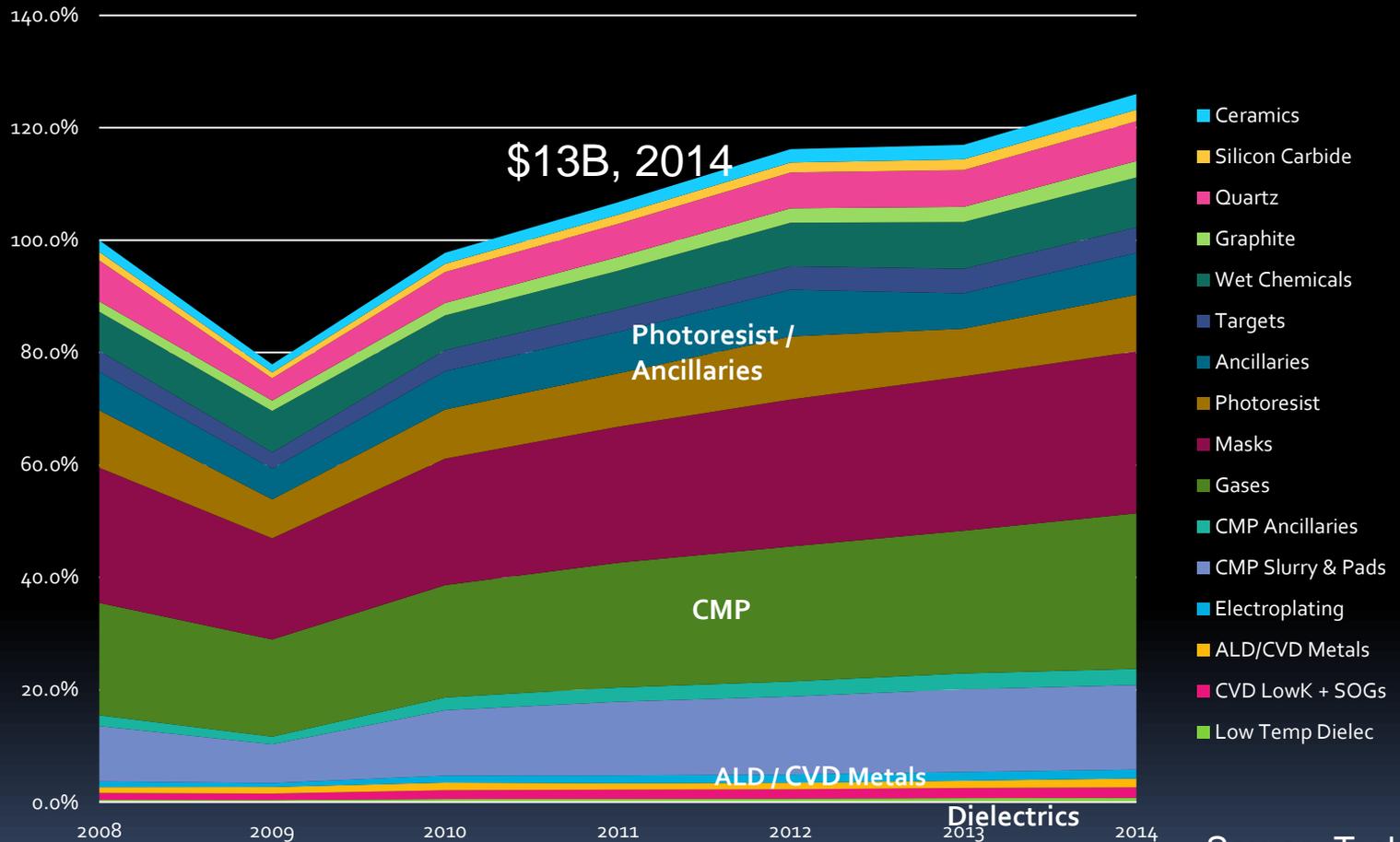L. Shon-Roy
K. Holland, PhD.
February 2015

Disclaimer

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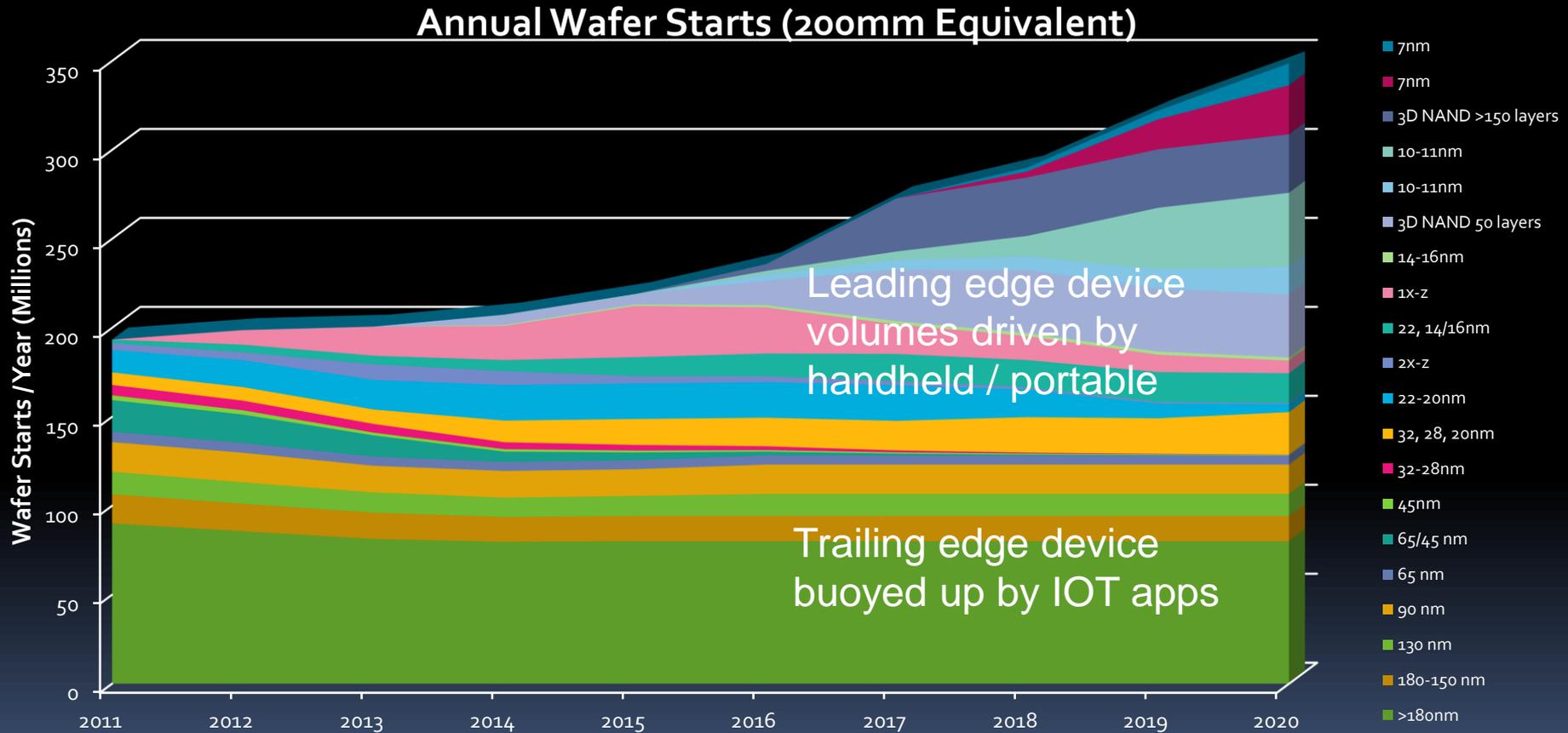
Yellowstone River, Montana

Outline

- Materials Overview

- Shifts to 3D

- MPU shift to 3D needs for new/more materials

  - Materials Opportunities / Forecasts

- Memory / NVM shift to 3D and impact on materials

  - Materials Opportunities / Forecasts

- Summary

WW Process Materials Forecast

$13B, 2014

Photoresist / Ancillaries

CMP

ALD / CVD Metals

Dielectrics

Legend:
- Ceramics
- Silicon Carbide
- Quartz
- Graphite
- Wet Chemicals
- Targets
- Ancillaries
- Photoresist
- Masks
- Gases
- CMP Ancillaries
- CMP Slurry & Pads
- Electroplating
- ALD/CVD Metals
- CVD LowK + SOGs
- Low Temp Dielec

Source: Techcet

# Forecast of IC Trends by Node and Product Type, includes R&D (200mm equivalent utilized wafers/year)

Annual Wafer Starts (200mm Equivalent)

Leading edge device volumes driven by handheld / portable

Trailing edge device buoyed up by IOT apps

Legend:
- 7nm
- 7nm
- 3D NAND >150 layers
- 10-11nm
- 10-11nm
- 3D NAND 50 layers
- 14-16nm
- 1x-z
- 22, 14/16nm
- 2x-z
- 22-20nm
- 32, 28, 20nm
- 32-28nm
- 45nm
- 65/45 nm
- 65 nm
- 90 nm
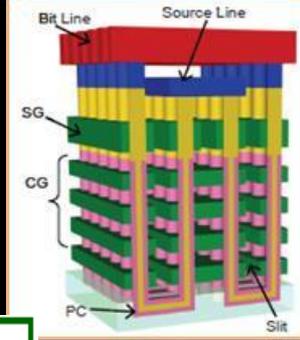- 130 nm
- 180-150 nm
- >180nm

Source: Techcet and SEMI

IC Technology Roadmap Evolutions/Revolutions

Note "Node" is "nm" performance, physical is GLph
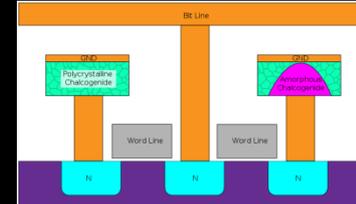
Non-Volatile 1X & 1Z nm Shrink Planar NAND
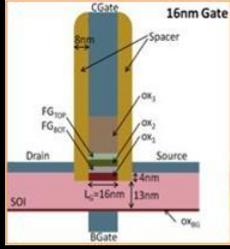
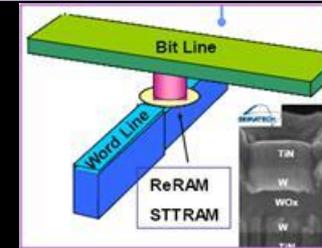**Non-Volatile 80-30nm features 3D NAND (BiCS, TCAT, etc.)**

Charge Trap Flash in Vertical Plane also called 3D or V-NAND

Non-Volatile <10nm CNT? PCM

3D/V-NAND Extend for 5+ yrs with 16 to 256 layers

RAM & Non Volatile ? 18-15nm STT-MRAM

DRAM 32-28nm Vertical Capacitors

DRAM 26-16nm HκMG + Si Fin

Continue DRAM Shrink w/ MPU

Saddle Fin FET
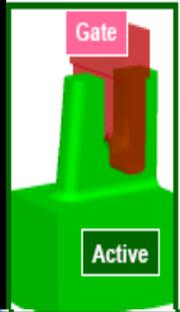
7nm III-V or Ge ?

10nm Fin w/ STI, channel change?
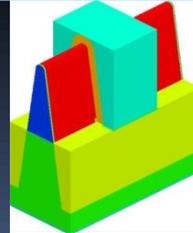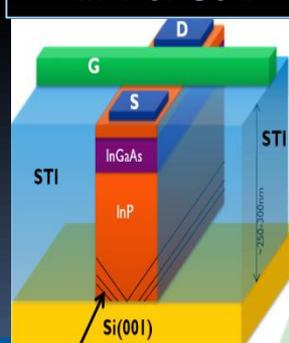
EUV 7nm ?

14nm TriGate 14/16nm FinFET-STI

20nm Planar SOI Hκ/MG

450mm 7nm?

2014 to 2019 Technologies Opportunities

- MPU
  - Multi-patterning Dielectrics will be used for smallest dimension features <28nm
  - High k Gate Dielectric used with Metal Gate Electrode
- DRAM – 1X, 1Z
  - Aggressive scaling, requiring more multipatterning
- Flash
  - 2D - 16nm gates requiring more multipatterning
  - Transition to 3D NAND similar challenges to MPU for 3D structures but with larger design rules, > 20nm.
- More/Better: MP Dielectrics, Cleans, litho, ALD

Advanced Transistor Channel Implications

FinFET with STI and non-implant Si Doping

Ge or III-V?   TFET. GAA or STT?
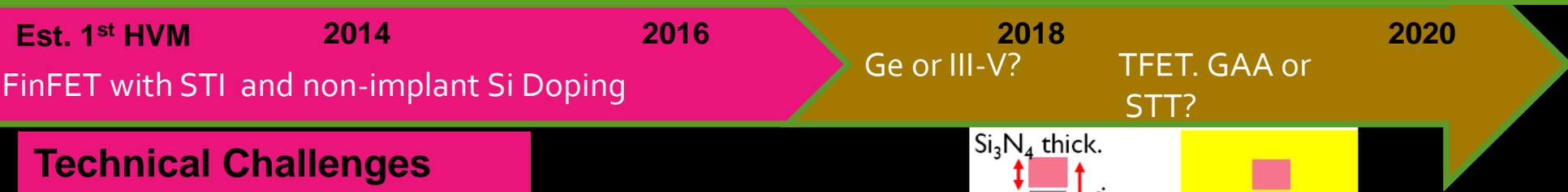
Technical Challenges

FinFET Formation
  Adequate Hard Mask
  Si Etch Profile for 2 Step-Etch
  Si Fin Surface Roughness & Damage
  Etch Residues
  Post Etch Cleans w/o Defects or Pattern Damage

Uniform "In Situ" Si Fin Doping / Strain
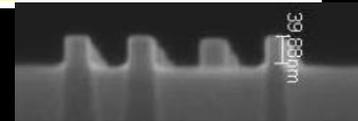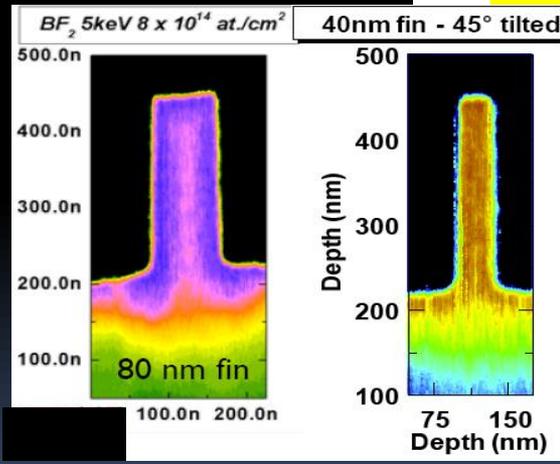 **Doping Uniformity Profile Analyses**

STI / Gapfill Dielectrics – More Spin on?

Need for More and Better
- Multipatterning Dielectrics and Cleans, selective etchants

Need for More
- Photoresist and ALD processes

Si₃N₄ thick. / Trench dep. / STI thick. / Fin height / Fin

BF₂ 5keV 8 x 10¹⁴ at./cm²   40nm fin - 45° tilted
80 nm fin
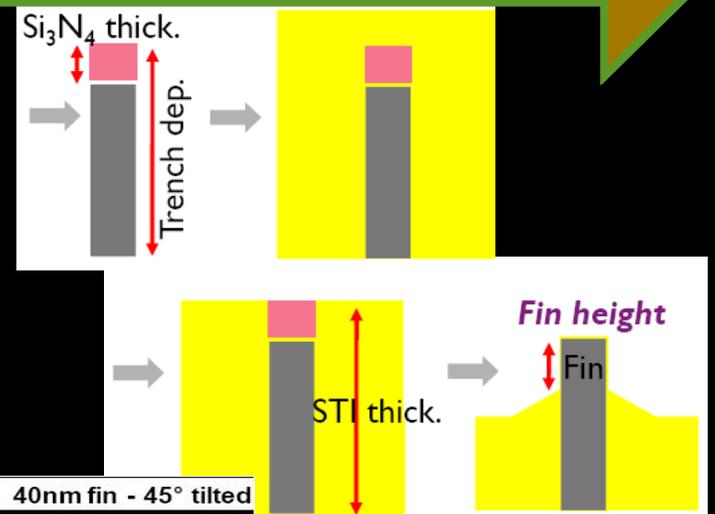
Composite from numerous publications with roadmaps

More and More Advanced Cleans ($)

Cleaning Chemicals

$2.5B

$381M

190M

| | 2000 | 2005 | 2010 | 2015 | 2020 |

■ Basic Wet Chemicals ■ Basic Solvents (i.e. IPA) ▣ Specialty Residue Removers ■ PR Strippers (TMAH)
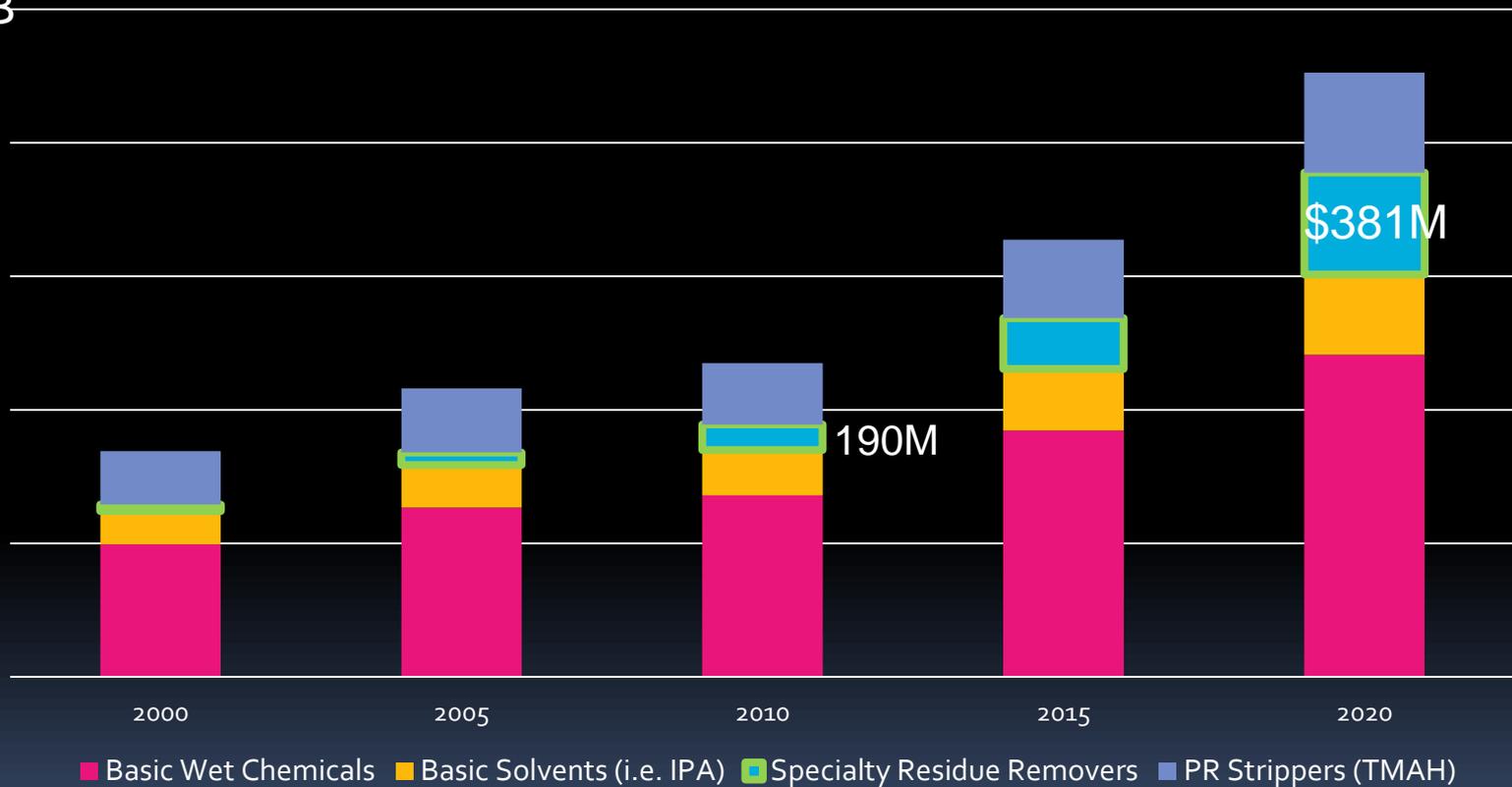
Source: Techcet

Source: Techcet Group

Advanced Lithography Implications

Est. 1st HVM	2014	2016	2018	2020
Litho 193i SIT	Dbl & Quad Patterning	& Self Assembly	& EUV ?	

Cost, Control & Reproducibility

Without EUV
   Sidewall Image Transfer (SIT)
      Deposition and Etch-Back Control

   Double/Quad Patterning
      Multi Litho - incr Dep, Etch, Strip
      2-4 X Photoresist Materials
      Etch CD Control
      Dep Coverage Uniformity
      Cleans: Particle and Damage Free
      CD, Overlay & Defect Metrology

   Directed Self Assembly
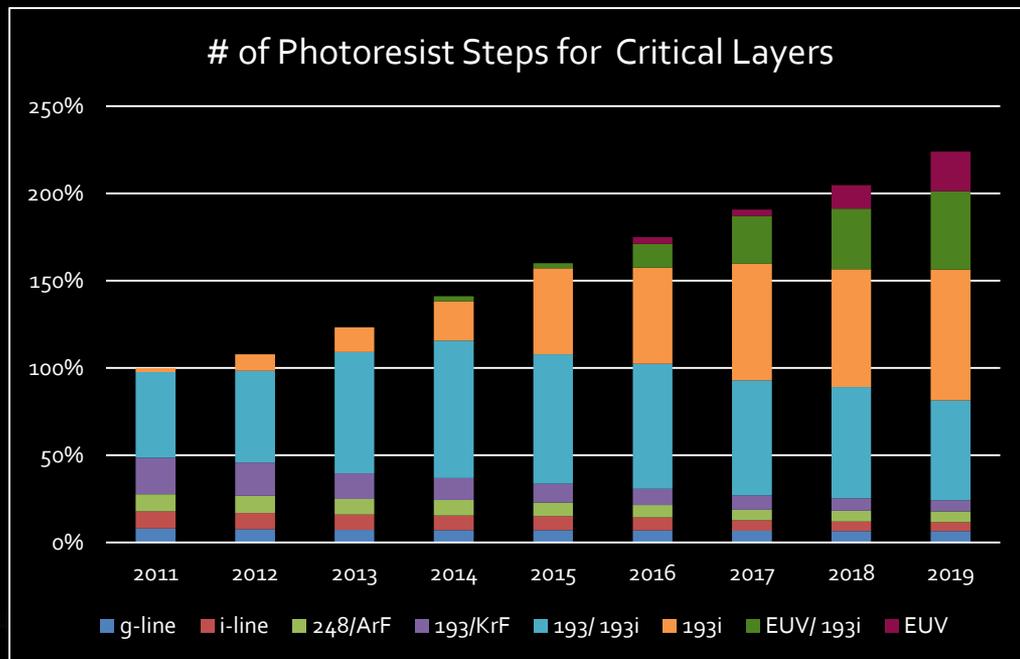   **Specific Location / Geometry Patterns**
      Metrology and Defect Analyses before Develop

EUV (first planned for 32nm, now expected <"10nm Node")
   Masks Detecting, Controlling & Repairing Defects
   Improved Exposure Dose for Throughput
   EUV Multi Patterning required for smallest features

# of Photoresist Steps for Critical Layers

Legend: g-line, i-line, 248/ArF, 193/KrF, 193/ 193i, 193i, EUV/ 193i, EUV

Source: Techcet Group

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Feb 2015

Advanced Lithography Implications

| Est. 1ˢᵗ HVM
Litho 193i SIT | 2014
Dbl & Quad Patterning | 2016
& Self Assembly | 2018
& EUV ? | 2020 |

Photoresist Critical Layers

EUV not only will allow for finer resolution lithography but aid in reducing the number of litho exposures.

(bar chart: Photoresist Critical Layers, y-axis 0%–250%, x-axis years 2011–2019)

- without EUV
- with EUV

Legend: g-line ■ i-line ■ 248/ArF ■ 193/KrF ■ 193/ 193i ■ 193i ■ EUV/ 193i ■ EUV ■
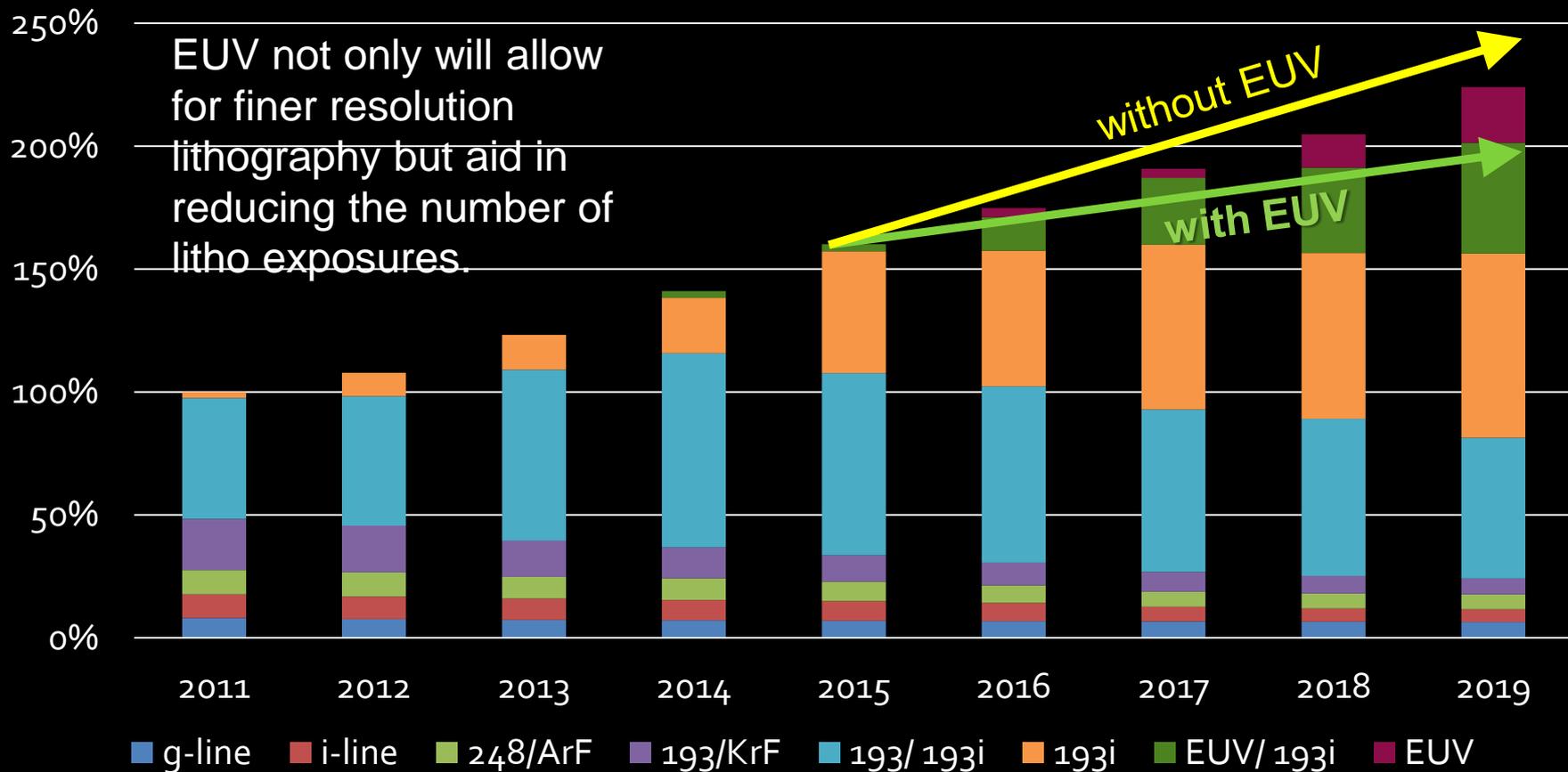
Hi K /ALD History & Forecast

ALD/CVD High k & Metal Precursors

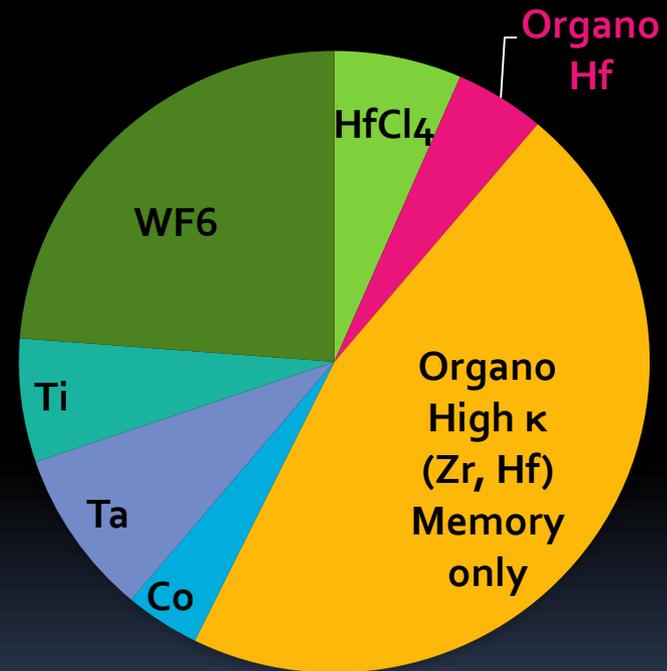- Interconnect — $200M
- Logic Front End (HkMG) — $150M
- Memory High k — $75M
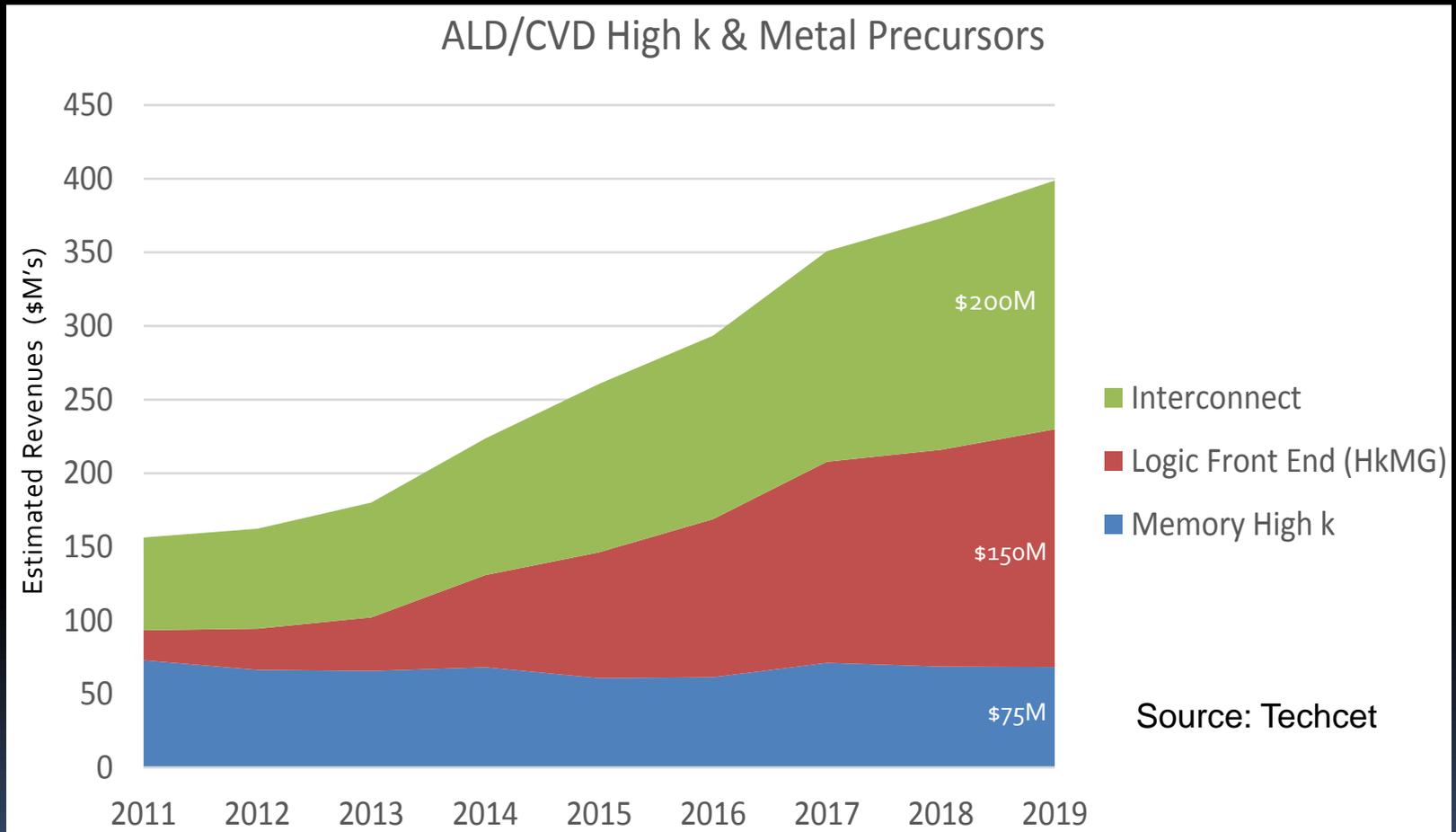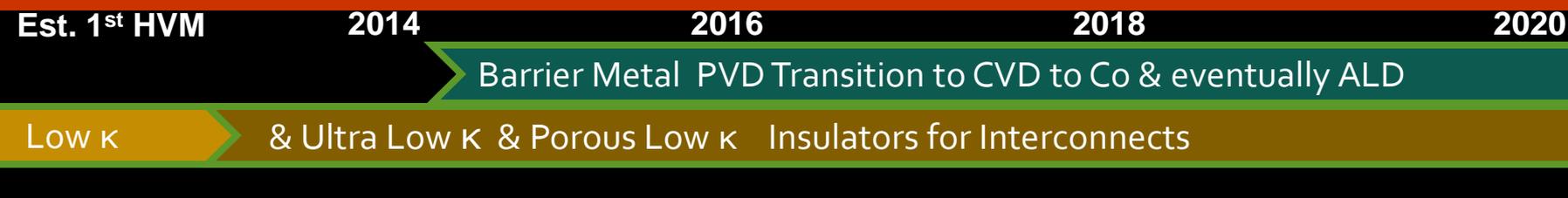
Source: Techcet

Hi K /ALD Metal Precursors

- 2014 Metal / Metal Oxide Precursors market ~ $225M

- Expected to be ~$400M by 2019

- Front end precursors dominate this space.

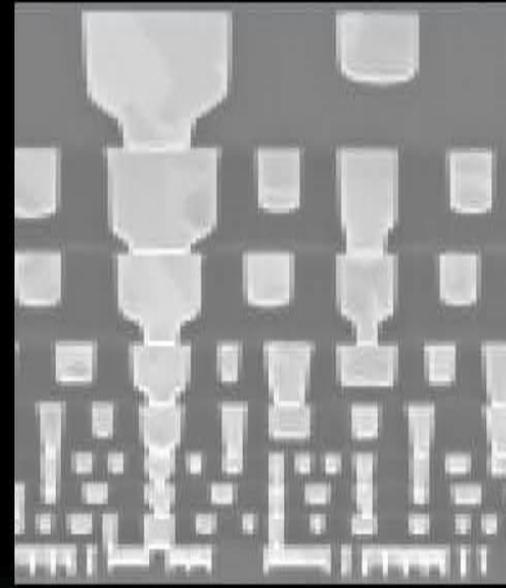Hi K /ALD Metal Precursors as a % of total 2014 revenues

- Organo Hf
- HfCl$_4$
- WF6
- Ti
- Ta
- Co
- Organo High κ (Zr, Hf) Memory only

Source: Techcet

Advanced MCU Interconnect Challenges/Opportunities

Est. 1st HVM	2014	2016	2018	2020

Barrier Metal PVD Transition to CVD to Co & eventually ALD

Low κ   & Ultra Low κ & Porous Low κ   Insulators for Interconnects
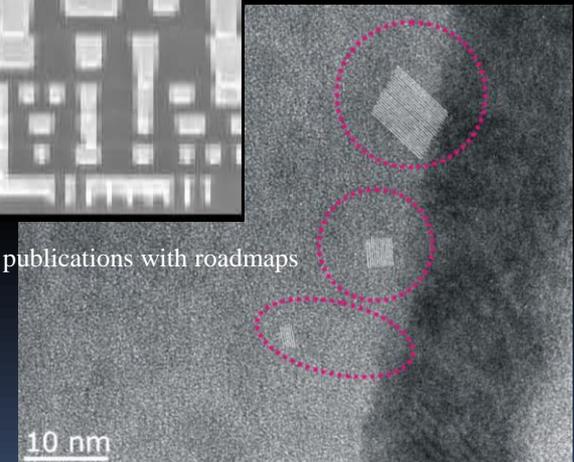
☐ **Cu Resistivity of Smallest Features**
Thin Effective <u>Barrier Metals</u>
CVD Ta self aligned Co?
Optimization of Cu Plating to Improve R_s

☐ **Ultra Low κ & Porous Low κ**
- Optimized Process & Materials
- Etch Profiles, Metal Diffusion into dielectric
- Reduce κ_{eff}
- Adequate Mechanical Strength

Composite from numerous publications with roadmaps

Note: There are 8 to 14 Metal Interconnect Levels for MPU. For new interconnect technologies, interconnect levels > 2x transistor process steps.

10 nm

TiN intrusion on unsealed porous LowK

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CMP Consumables

CMP Consumables

$2.5 B USD

Legend: Pads | Slurry | Pad Conditioners | PVA Brushes | Slurry Filters | P-CMP Clean Chemistries
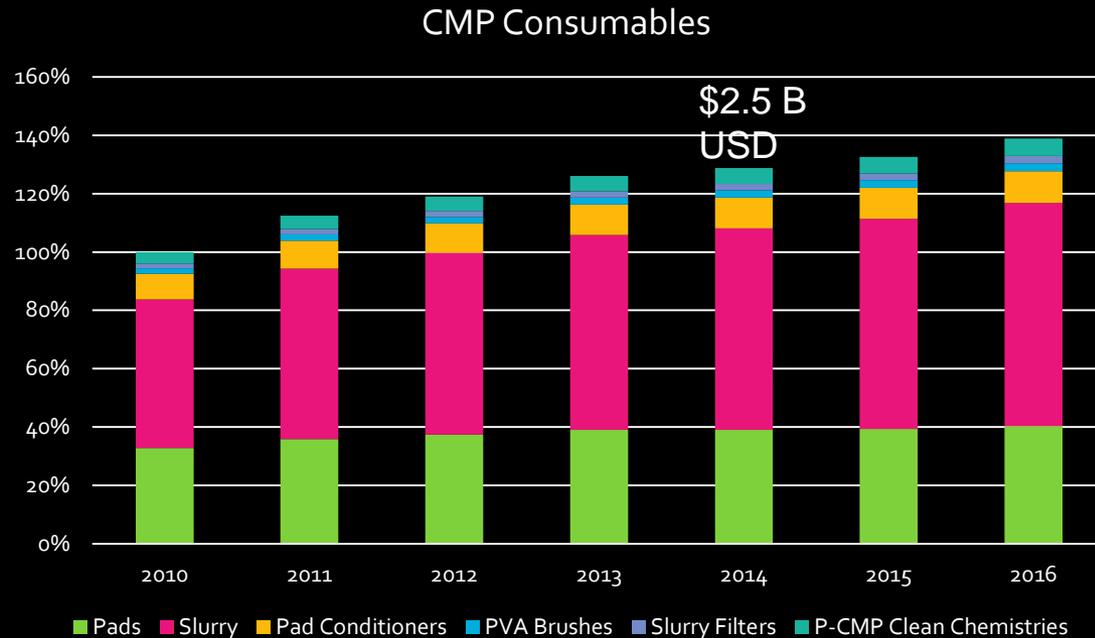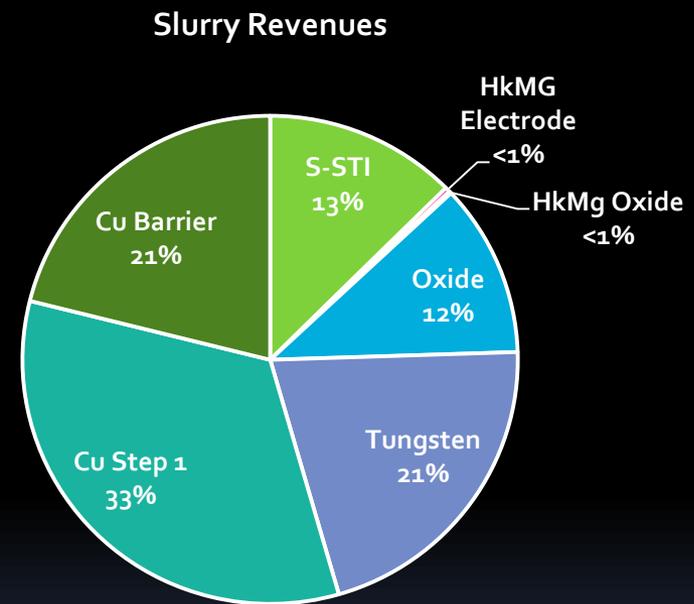
Source: Techcet

- Slurry is the fastest growing segment given that ASPs have held up relative to pad ASPs and Pad lifetime has improved over time.

Interconnect Layers and Materials driving CMP Consumables Revenues

- Coppper Slurry makes up for >50% of total slurry revenues

- Revenues total ~$1.3B

Slurry Revenues

Source: Techcet

Etch /Dep

This way to the Bastille

Key Challenges for 3D NAND

Non-Volatile Technology Status & Challenges 2014 to ~2018

- 2D NAND is going 3D. Every time they shrink, litho is a problem requiring more multipatterning litho i.e. for 1X and 1Z nodes

  - ~ 11nm on 2D can now be made w/ 20nm - 30nm on 3D.

- 3D NAND (2014 earliest shipments) --- pressing forward to higher density

  - >30nm lithography

  - Even More aggressive films control

  - Even More aggressive etching techniques

  - Even More defect & process control concerns

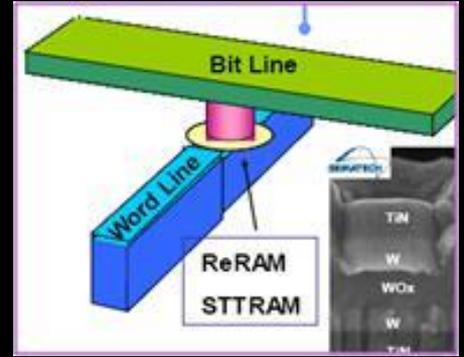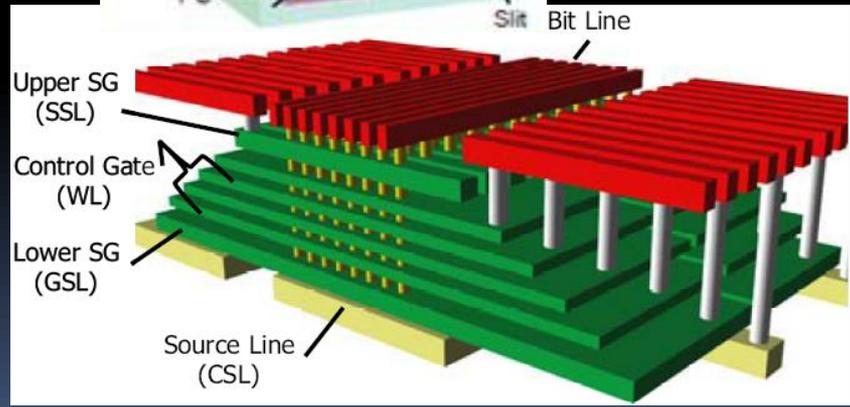 - Challenging defectivity & process control (e.g. etch depth)

Non-Volatile Technology Roadmap

Est. 1st Ship	2014	2015	2016	2017	2018

Non-Volatile >30 nm
3D NAND (BiCS, V-NAND, TCAT)

Extend for >5 yrs w/ more layers

Non-Volatile
1x – 1z NAND

CrossPoint
RAM & Non Volatile
STT-MRAM? CBRAM?
PCM? ReRAM (MVO)?
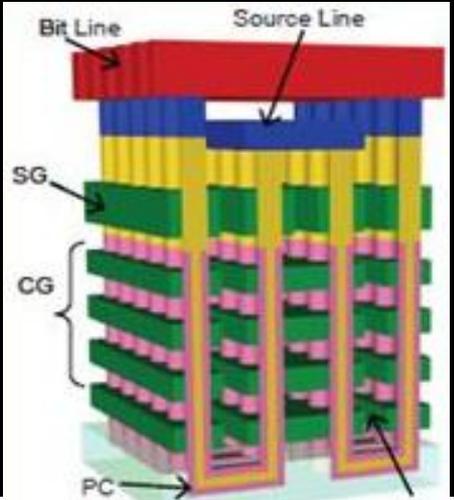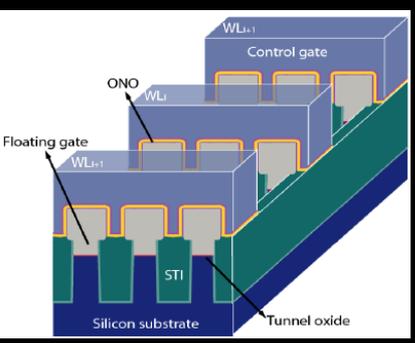
<10nm
CNT? PCM
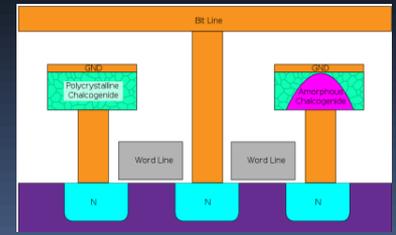
Composite from numerous publications with roadmaps

Material Implications- 3D/ V-NAND

from 18 - 32nm layers to 256 - 28nm layers

Etch / Cleans:
  Hard Mask for >70:1 Aspect Ratio
  Uniform Etch Thru Numerous Layers
  Cleans w/o Residues or Defects

Deposition (CVD/ALD):
  Difficult High AR Fills Ta_2O_5, TiN, W
  SiO_2, Si_3N_4

Defect Localization / Analysis Critical

NAND Challenge – Low Cost
  High Productivity Processes

No new device materials
  Ta_2O_5, SiO_2, Si_3N_4, PolySi, Ta, Ti, W, but
Possibly new cleaning/mixtures and hard mask materials

Composite from numerous publications with roadmaps

Channel Hole Etch
Creates non-functioning cells

Staircase Etch
Causes cell cross talk

Step 1: Partial fill deposition

Step 2: Extreme step shapes W film, maintains opening, smoothes W film

Step 3: Deposit complete-void free fill
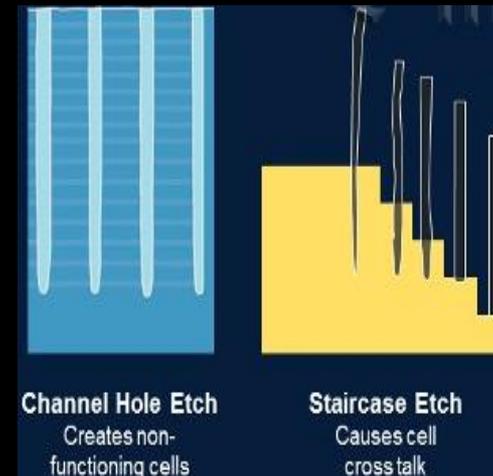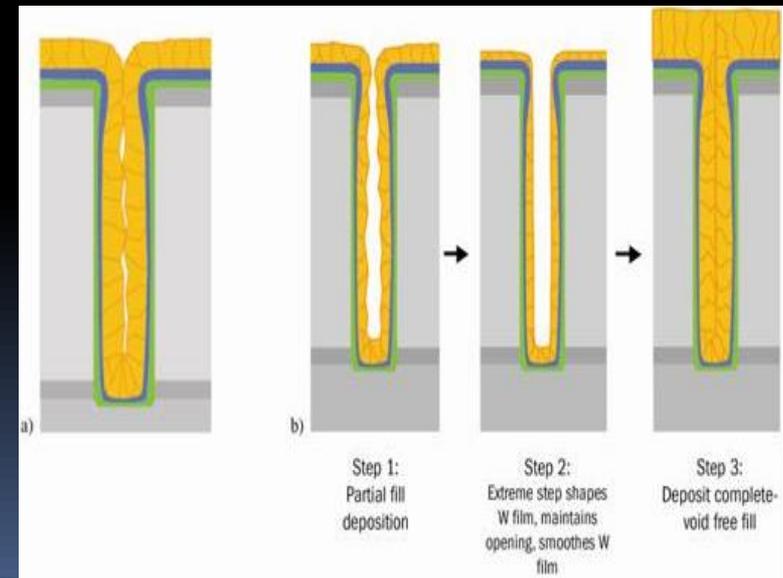
Multi-Patterning Precursors: Dielectrics

Multi-patterning Precursor Volumes

$73M

Legend: ■ DP Precursors   ■ QP+ Precursors

Source: Techcet Group
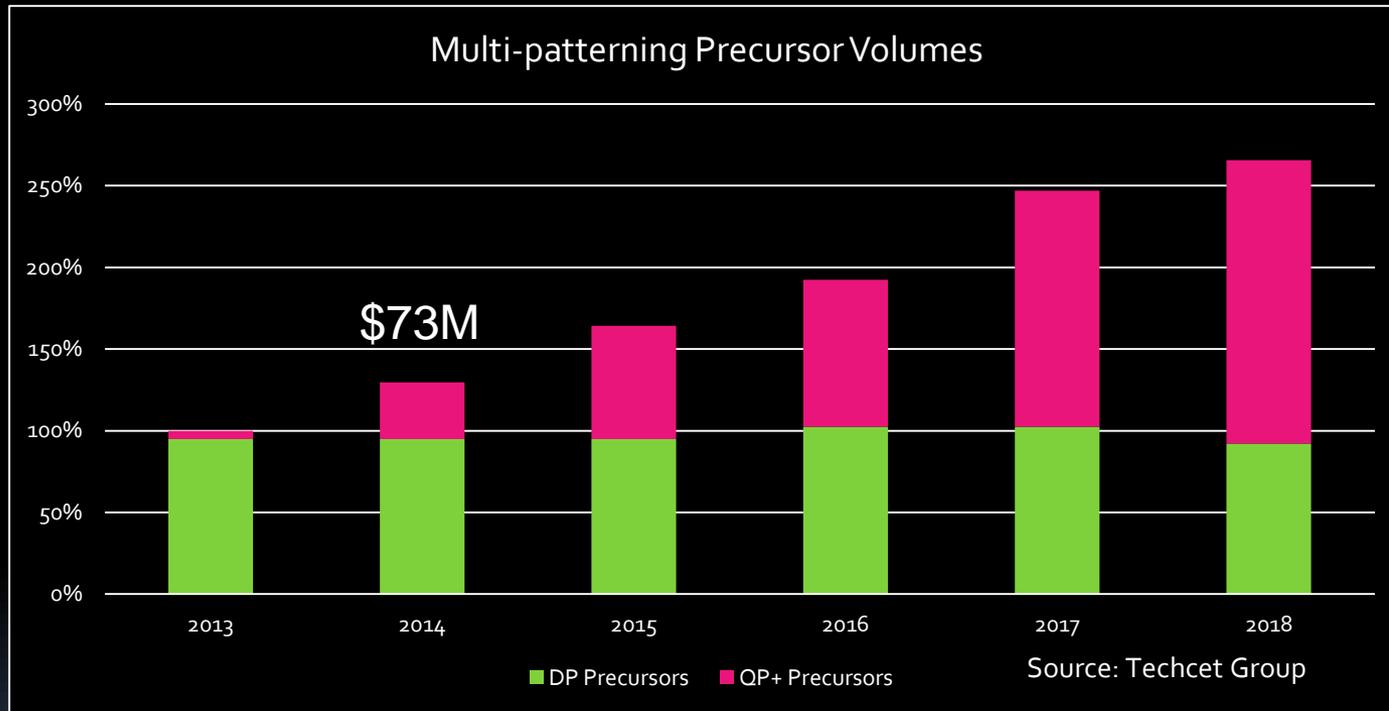
Source: Techcet

- Driven by need for finer line widths w/ or w/o EUV

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Specialty Gases

- An increase in multi-patterning and inter-connect layers drives the need for more electronic specialty gases.

- Total Etch Gases > $180M

- Multi-patterning precursors >$70M

- Low temp precursors for patterning and gapfill being sought after

2015 est.

Pie chart segments:
- Ambient Gas Mixtures 4%
- High K 4%
- WF6 4%
- NF3 13%
- Low K 9%
- Other Gases & Others (i.e. AHM gases, HCl, SF6, H2S/H2Se, etc.)…
- CF Gases 6%
- SiH4 22%
- Liquide Dopants and TEOS 4%
- Ion implant SDS & Cylinder 10%
- GeH4 3%
- NH4 7%
- N2O 4%
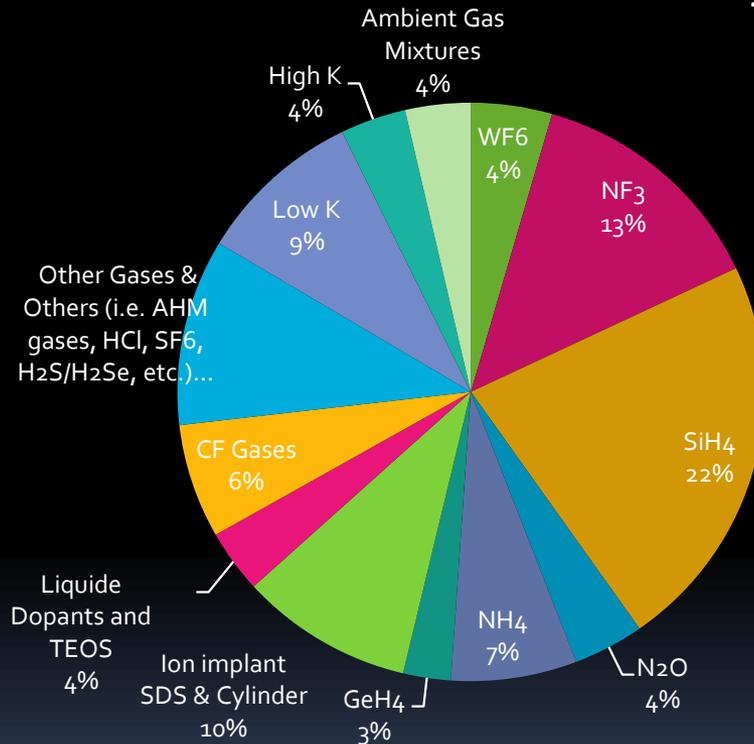
Source: Techcet

2015 – 2019 Materials Summary

- Increased use of ALD and Hi K / ALD materials although no new materials until 2019 or beyond.

- Increased use of and better gapfill / STI materials

- Multi-patterning will continue through all technology nodes, driving need for
  - better hard mask materials, > 2X in volume in 3yrs
  - Incr. vol. usage of photoresist - 10%+
  - Incr. vol. and new blends of specialty cleaning $381M by 2020.

- Interconnect layers will continue to grow, driving
  - Porous low K
  - More ALD barriers, More CMP Consumables
- Packaging Opportunities – TSV and WLP

Other Materials for 2019 and Beyond?

- Logic
  - Transition Si to Higher Mobility Channels at 7nm (less likely at 10nm), i.e. Ge or III-V
  - EUV resists + Multi-Patterning, Directed Self Assembly
  - Higher k Gate Dielectric and Different Metal Gate Electrode
- Memory
  - A variety of new materials will be needed to support new device technologies
    - PCM , CNT, STT, ReRAM , RedOx, ...etc.

www.Techcet.com

Where to get more detailed information?

Techcet's
Critical Materials Report on
High k & Metal CVD/ALD
Precursors

Where to get more information on Materials?

www.Techcet.com

- CMP Consumables & Ancillaries
- Gases (Spec. & Bulk)
- ALD / Hi K Metal Precursors
- Photoresists
- ARCs & PR Ancillaries
- Metals – Targets, Conductive Inks/Pastes
- Wafer Mfg Consumables
- Wet Chemicals

- Advanced Cleaning
- Equip't Consumables -
    - Quartz
    - Graphite
    - Silicon Carbide
    - Ceramics
    - Silicon
- Silicon Wafers/Polysilicon
- Others

Materials Markets, Technology and Supply Chain Expertise

Acknowledgements

- **SEMI – H.D. Cho and Dan Tracy, Ph.D.**
- **VLSI Research - Risto Puhakka**
- **Sematech - Critical Materials Council**
- **Techcet Group Analysts**

Techcet Group (+ Experience listing)

- **Lita Shon-Roy – President / CEO**
  - Rasirc/Matheson Gas, IPEC/Athens, Air Products, Rockwell/Brooktree
- **Karey Holland, Ph.D. – Chief Technical Officer**
  - FEI, NexPlanar, IPEC, Motorola, IBM
- **Chris Michaluk – Director of Business Development & Sr. Analyst**
  - H.C. Stark, Climax Molybdenum, Williams, Cabot SuperMetals
- **Sue Davis – Business Development Manager & Sr. Analyst**
  - TI, Sematech, Motorola, Rodel (DOW)
- **Bruce Adams – Sr. Technology Analyst**
  - Matheson Gas, Air Products, & Chemicals, Honeywell
- **Yu Bibby, Ph. D. – Sr. Technology Analyst**
  - UV Global, ipCapital Group, Wilkes University
- **Jiro Hanaue – Sr. Technology Analyst**
  - Applied Materials
- **Ralph Butler – Technology Analyst**
  - Sun Edison / MEMC, ATMI
- **Mike Fury, Ph.D. – Sr. Technology Analyst**
  - IBM, Rodel, EKC, Vantage
- **Chris Blatt – Sr. Market Analyst**
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Thank you!

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