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Electronics Materials Information

THE IMPACT OF 3D-DEVICES ON THE FUTURE OF PROCESS MATERIALS - TRENDS & OPPORTUNITIES

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Materials Examples

- Process materials used to make semiconductor devices
  - Gases – etching, doping
  - Wet chemicals – cleaning / Residue removal
  - CMP Consumables
  - Metals – sputter targets, CVD/ALD precursors
  - Dielectric Precursors – low K / high K
  - Wafers
  - Etc.

Outline

- Device Technology Metamorphasis to 3D
- MPU shift to 3D needs for new/more materials
  - Materials Opportunities / Forecasts
- Memory / NVM shift to 3D and impact on materials
  - Materials Opportunities / Forecasts
- Ripe Opportunities Summary

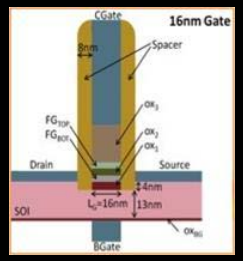
Disclaimer

- This presentation represents the interpretation and analysis of information generally available to the public or released by responsible agencies or individuals. Data was obtained from sources considered reliable. However, accuracy or completeness is not guaranteed. This report contains information generated by Techcet by way of primary and secondary market research methods.

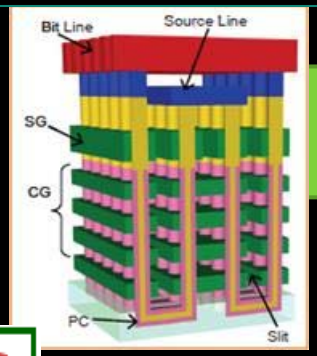
IC Technology Roadmap Evolutions/Revolutions

Note “Node” is “nm” performance, physical is GLph

Non-Volatile 1X & 1Z nm Shrink Planar NAND



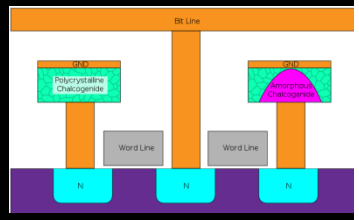
Non-Volatile 80-30nm features 3D NAND (BiCS, TCAT, etc.)



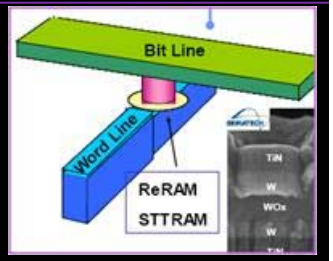
Charge Trap Flash in Vertical Plane also called 3D or V-NAND

3D/V-NAND Extend for 5+ yrs with 16 to 256 layers

Non-Volatile <10nm CNT? PCM



RAM & Non Volatile ? 18-15nm STT-MRAM

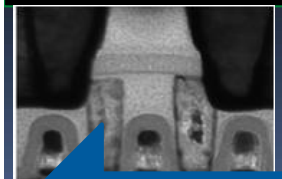


DRAM 32-28nm Vertical Capacitors

DRAM 26-16nm HκMG + Si Fin

Continue DRAM Shrink w/ MPU

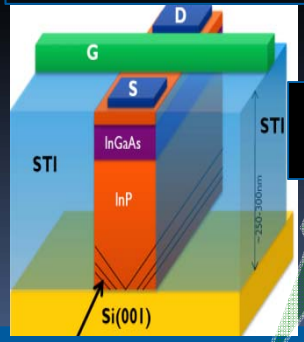
20nm Planar SOI Hκ/MG



14nm TriGate 14/16nm FinFET-STI

10nm Fin w/ STI, channel change?

7nm III-V or Ge ?



EUV 7nm ?

450mm 7nm?

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2013 — 2014 — 2015 — 2016 — 2017 — 2018 — 2019

2014 to 2019 Technologies Opportunities

- MPU
  - Multi-patterning for smallest dimension features <28nm
  - High k Gate Dielectric used with Metal Gate Electrode
- DRAM – 1X, 1Z
  - Aggressive scaling, requiring more multipatterning
- Flash
  - 2D - 16nm gates requiring more multipatterning
  - Transition to 3D NAND similar challenges to MPU for 3D structures but with larger design rules, > 20nm.
- More/Better: MP Dielectrics, Cleans, litho, ALD

Advanced Transistor Channel Implications

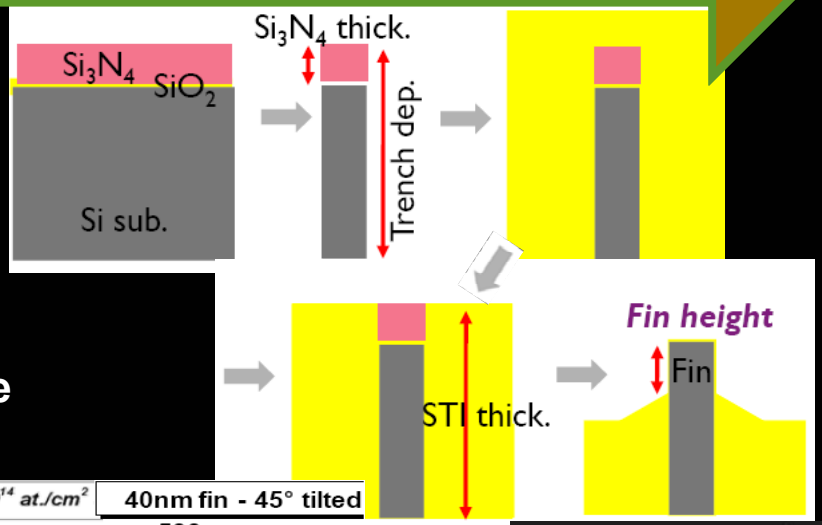
Est. 1st HVM	2014	2016	2018	2020
FinFET with STI and non-implant Si Doping			Ge or III-V?	TFET. GAA or STT?

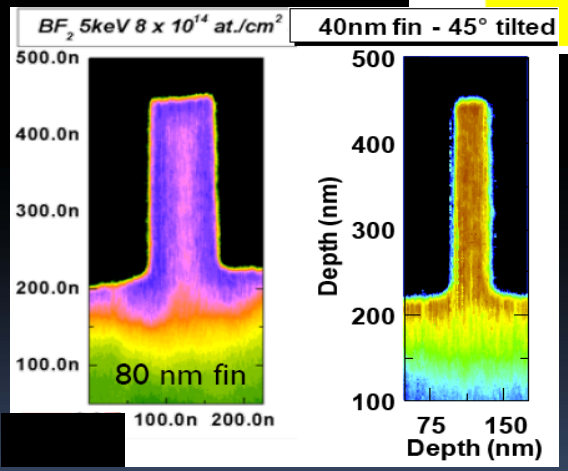
Technical Challenges

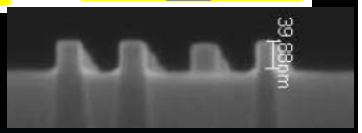
FinFET Formation
- **Adequate Hard Mask**
- **Si Etch Profile for 2 Step-Etch**
- **Si Fin Surface Roughness & Damage**
- **Etch Residues**
- **Post Etch Cleans w/o Defects or Pattern Damage**

Uniform "In Situ" Si Fin Doping / Strain
- **Doping Uniformity Profile Analyses**

STI / Gapfill Dielectrics – More Spin on?







Composite from numerous publications with roadmaps

Need for More and Better
- Multipatterning Dielectrics and Cleans, selective etchants

Need for More
- Photoresist and ALD processes

Advanced Lithography Implications

Est. 1st HVM Litho 193i SIT | **2014** Dbl & Quad Patterning | **2016** & Self Assembly | **2018** & EUV ? | **2020**

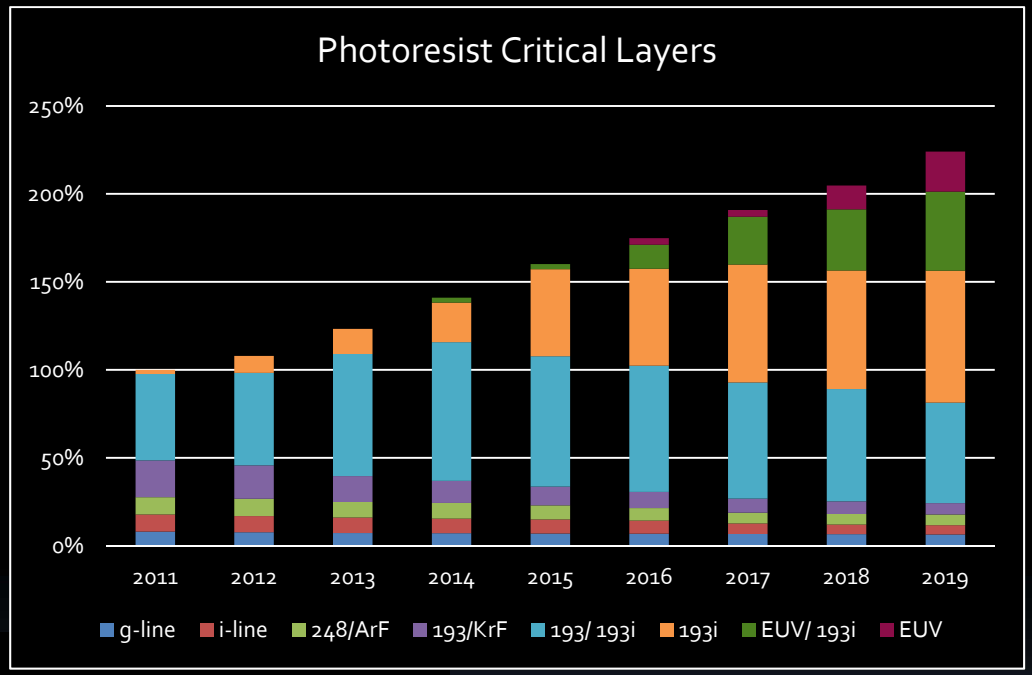
Cost, Control & Reproducibility

Without EUV

- **Sidewall Image Transfer (SIT)**
  - **Deposition and Etch-Back Control**
- **Double/Quad Patterning**
  - **Multi Litho - incr Dep, Etch, Strip**
  - **2-4 X Photoresist Materials**
  - **Etch CD Control**
  - **Dep Coverage Uniformity**
  - **Cleans: Particle and Damage Free**
  - **CD, Overlay & Defect Metrology**
- **Directed Self Assembly**
  - **Specific Location / Geometry Patterns**
  - **Metrology and Defect Analyses before Develop**

EUV (first planned for 32nm, now expected <"10nm Node")

- **Masks Detecting, Controlling & Repairing Defects**
- **Improved Exposure Dose for Throughput**
- **EUV Multi Patterning required for smallest features**



Source: Techcet Group

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Advanced MCU Interconnect Challenges/Opportunities

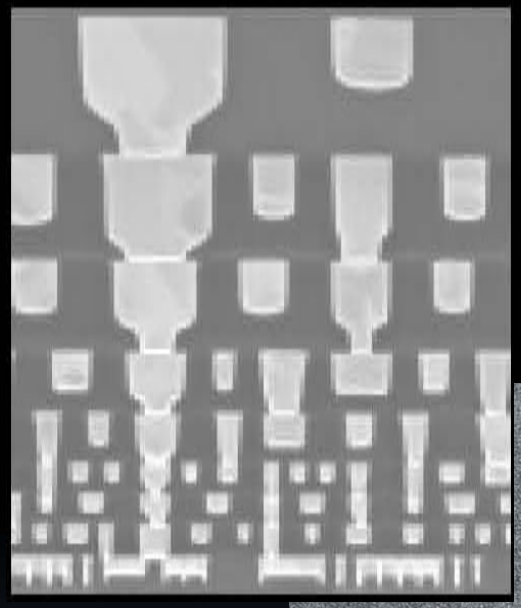
Est. 1st HVM | 2014 | 2016 | 2018 | 2020

Barrier Metal PVD Transition to CVD to Co & eventually ALD

Low κ & Ultra Low κ & Porous Low κ Insulators for Interconnects

- **Cu Resistivity of Smallest Features**
  Thin Effective Barrier Metals
  CVD Ta self aligned Co?
  Optimization of Cu Plating to Improve R_s

- **Ultra Low κ & Porous Low κ**
  - Optimized Process & Materials
  - Etch Profiles, Metal Diffusion into dielectric
  - Reduce κ_{eff}
  - Adequate Mechanical Strength



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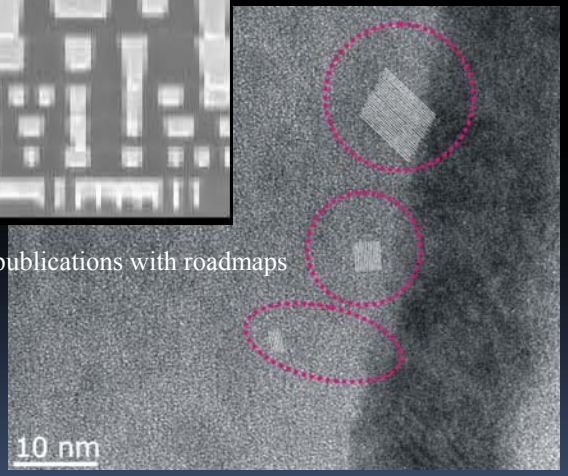
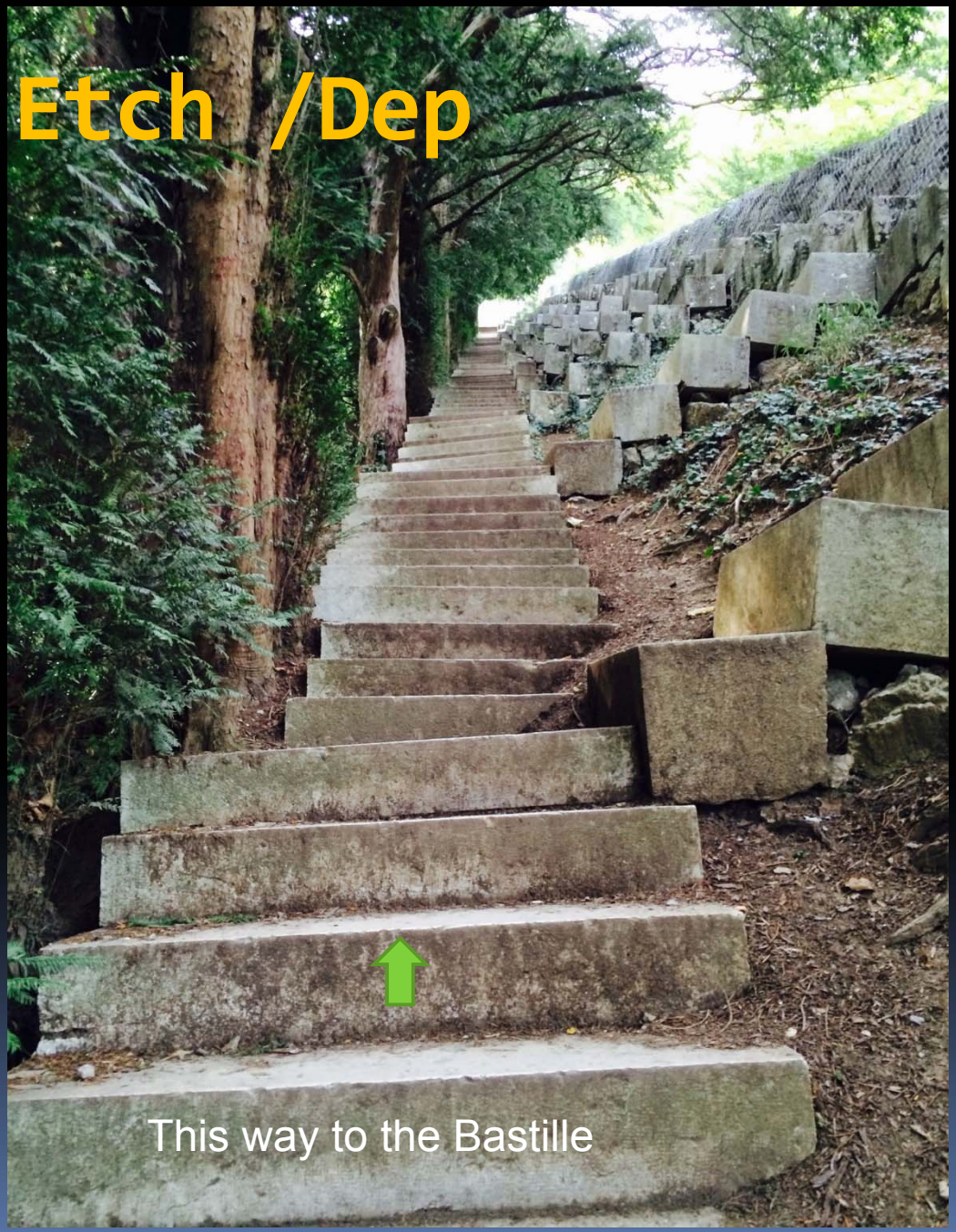


TiN intrusion on unsealed porous LowK

Note: There are 8 to 14 Metal Interconnect Levels for MPU. For new interconnect technologies, interconnect levels > 2x transistor process steps.

Key Challenges for 3D NAND



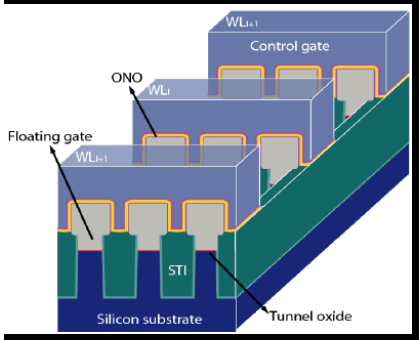
2014 to ~2018 Non-Volatile Technologies

- To achieve smaller foot print devices NAND is going 3D. What was approaching 11nm can now be 20nm - 30nm with 3D.
- More defect & process control concerns
  - Even More aggressive films control (deposition)
  - Even More aggressive etching techniques
  - Need for More effective residue removal
- 3D NAND (2014 earliest shipments) --- pressing forward to higher density, 50 to > 150 layers leading to higher AR and etch/dep challenges

Non-Volatile Technology Roadmap

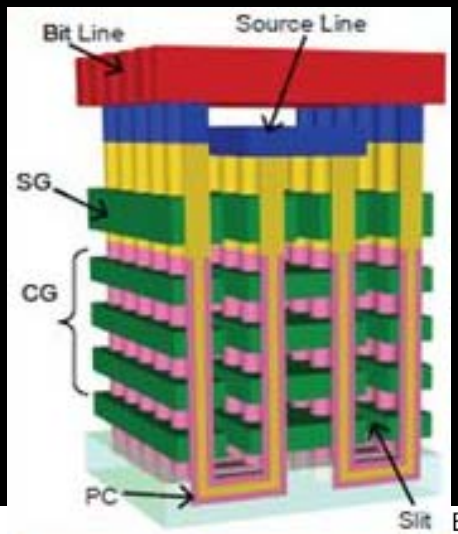
Est. 1st Ship	2014	2015	2016	2017	2018

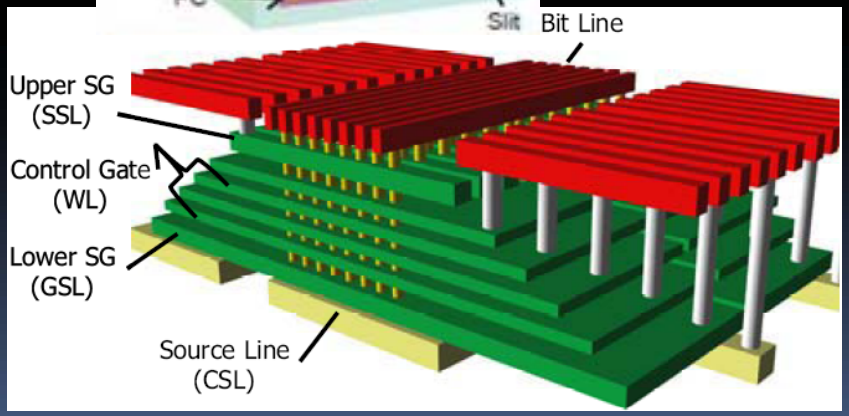
Non-Volatile
1x – 1z NAND



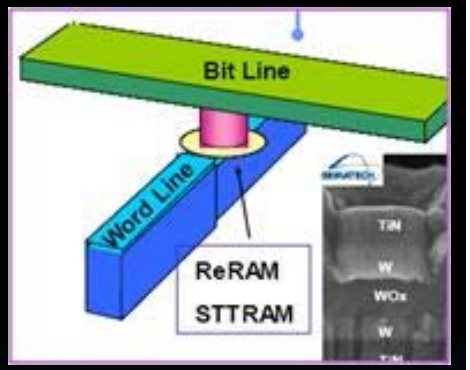
Non-Volatile >30 nm
3D NAND (BiCS, V-NAND, TCAT)

Extend for >5 yrs w/ more layers

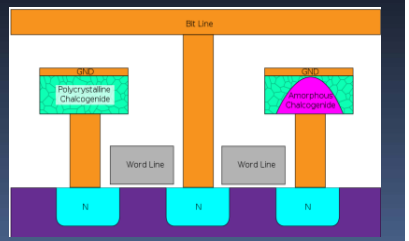




CrossPoint
RAM & Non Volatile
STT-MRAM? CBRAM?
PCM? ReRAM (MVO)?



<10nm
CNT? PCM



Composite from numerous publications with roadmaps

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Ripe Opportunities Summary

- Continued need to shrink driving
  - FLASH to go 3D
  - DRAM to go to FINFET for sub 20nm devices
  - MPUs to integrate FINFETs for 22nm devices
- Increased use of ALD and Hi K / ALD materials although no new materials until 2019 or beyond.
- Increased use of and better gapfill / STI materials
- Multi-patterning will continue through all technology nodes, driving need for
  - better hard mask materials, > 2X in volume in 3yrs
  - increased volume usage of photoresist - 10%+
  - Increased volume and new blends of specialty cleaning chemistries; $381M by 2020.
- Interconnect layers will continue to grow
  - Porous low K
  - More ALD barriers, More CMP Consumables

Other Materials for 2019 and Beyond?

- Logic
  - Transition Si to Higher Mobility Channels at 7nm (less likely at 10nm), i.e. Ge or III-V
  - EUV resists + Multi-Patterning, Directed Self Assembly
  - Higher k Gate Dielectric and Different Metal Gate Electrode
- Memory
  - A variety of new materials will be needed to support new device technologies
    - PCM , CNT, STT, ReRAM , RedOx, …etc.

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Thank you!

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